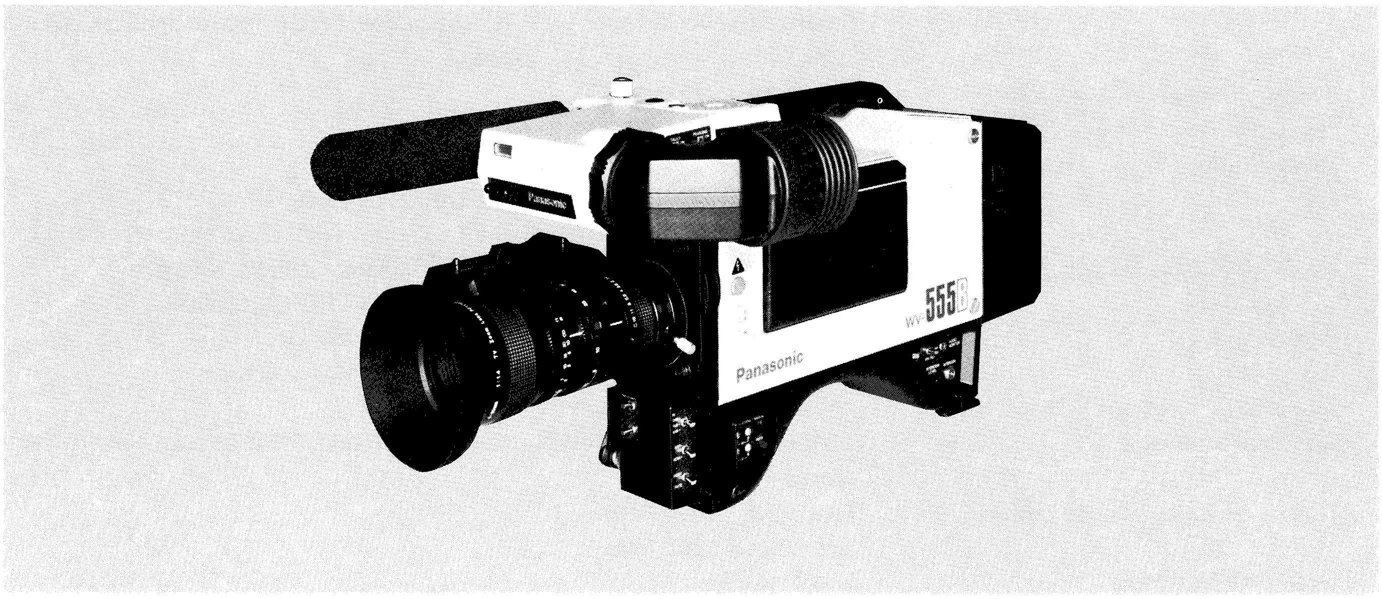
ORDER NO. VKD85030902C8

Service Manual

Colour Video Camera

WV-555B Series



o This WV-555B series service manual only includes different portion from WV-555 series service manual.
o Please file this service manual with WV-555 series service manual (Order No. VKD83100784C8).

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Panasonic

Matsushita Electric Trading Co., Ltd.
P.O. Box 288, Central Osaka Japan

SPECIFICATIONS

ENG Colour Camera WV-555BX

Pick-up System :	Middle index prism system using three SATICON™ tubes
Pick-up Tube :	Three 1/2"-scan electrostatic focusing, magnetic deflection SATICON™ tube, type H4111
Scanning Standard :	625 lines, 50 fields, 25 frames
Synchronizing System :	Internal or external (gen-lock) switchable automatically Internal : PAL standard External (gen-lock) Input : PAL composite (VBS) signal or black burst signal
Subcarrier Phase for Gen-Lock :	Adjustable more than 360°
Horizontal Phase for Gen-Lock :	Adjustable from −0.1 μsec to +3.5 μsec
Video Output :	Two outputs 1.0Vp-p PAL composite/75 ohms x 1 (BNC connector) 1.0Vp-p PAL composite/75 ohms x 1 (32-pin VTR/RCU connector)
Monitoring Video Output (Pix Output) :	R-G or B-G composite signal selectable/75 ohms x 1 (BNC connector)
Auxiliary Input :	1.0 Vp-p composite/75 ohms through 32-pin VTR/RCU connector
Audio Input :	Mic Input : -72 dBm x 1 (XLR type connector)
Audio Output :	-20 dBm or -72 dBm switchable (32-pin VTR/RCU connector)
Illumination Required :	140 footcandles(1400 lux) at F2.8
Signal-to-Noise Ratio :	51 dB (luminance) at 140 footcandles(1400 lux), F2.8 without gamma and aperture correction
Horizontal Resolution (at center) :	PAL signal : 550 lines Green signal : 600 lines
Geometric Distortion :	Less than 2%
Sweep Linearity :	Less than 2%
Registration :	Less than 0.1% within circle having a diameter 80% of picture height Less than 0.3% within circle having a diameter of picture height Less than 0.6% elsewhere
Vertical Enhancer :	Standard : 2-line type
White Balance :	Automatic
Black Balance :	Automatic
Centering for Registration :	Automatic or manual
Feedback(Automatic) Beam Control :	2 F-stop (4 times)
Colour Bar :	EBU colour bar generator
Colour Conversion Filters :	3200°K, 5600°K, 5600°K with 12.5% ND, close
Maximum Cable Length :	VTR Cable : 10m (30ft) 32-pin Studio Cable : 100m (300ft) with cable compensator
Switches :	Power, Standby, Colour Bar/Camera Selection, High Gain Selection, Auto White/Auto Black Set, Auto/Manual Centering Selection, Auto Centering Set, Monitor PIX Select, Level Indicator ON/OFF
Controls :	R and B vertical and horizontal centering, Intercom Level
Lens:	Option
Lens Mount :	Bayonet mount
Power Source :	12V DC five (5) ways such as; (1) Battery pack (2) AC adaptor (3) External DC through 4-pin external DC connector (4) VTR (external AC adaptor) (5) Remote control unit through 32-pin camera cable

TM : Trademark

Battery Pack Operating Time :		Approx. 1 hour with attached WV-PS37 Approx. 2 hours with optional WV-PS36
Power Consumption :	Camera Head :	18 watts (12V DC, 1.5A)
	ENG Configuration :	21 watts (12V DC, 1.75A)
	Studio Configuration :	32.4 watts (12V DC, 2.7A)
Ambient Operating Temperature :		14°F - 113°F (−10°C - +45°C)
Ambient Operating Humidity :		30% - 90%
Dimensions :	Camera Head Only ;	6-5/16"(W) x 10-1/8"(H) x 12-5/16"(D) 160(W) x 257(H) x 312(D) mm
	ENG Configuration ;	10-1/2"(W) x 10-1/8"(H) x 21"(D) 266(W) x 257(H) x 533(D) mm
	Studio Configuration ;	7-1/16"(W) x 16-15/16"(H) x 20-1/8"(D) 180(W) x 430(H) x 511(D) mm
Weight :	Camera Head Only ;	7.7 lbs (3.5 kg)
	ENG Configuration ;	14.3 lbs (6.5 kg)
	Studio Configuration ;	16.1 lbs (7.3 kg)

Weights and dimensions shown are approximate.
Weights and dimensions shown include optional zoom lens WV-LZ32/10.
Specifications are subject to change without notice.

1. CIRCUIT DESCRIPTION

o The comparison for circuit descriptions of WV-555B Series are described in the Table 1-1.

CIRCUIT DESCRIPTION	WV-555	WV-555B
1. Outline	A	A
2. Optics System	A	A
3. Pre-Preamplifier and Preamplifier Board	A	A
4. Process-1 Board	A	A
5. Process-2 Board	A	A
6. Encoder Board	A	A
7. Auto Board	A or S1	S1 or B
8. Sync Board	A	A
9. Detail Board	A	B
10. Deflection Board	A	A
11. High Voltage AIC Board	A	A
12. Mic Board	A	A
13. Mother Board	A	A
14. 1.5" Viewfinder	A	A

A : Original Service Manual for WV-555 (Order No. VKD83100784C8)
S1 : Supplement-1 Service Manual for WV-555 (Order No. VKD84060842S8)
B : Issued in this Service Manual for WV-555B

Table 1-1

1-1. Sync Board

The Sync board contains the following circuits.

1-1-1 Int 17MHz/14MHz Oscillator Circuit 3
1-1-2 Sync Generator Circuit 3
1-1-3 SC1 Out Circuit 4
1-1-4 SC2 Out Circuit 4
1-1-5 Sync Separation Circuit 4
1-1-6 Gen-Lock 14MHz Oscillator Circuit 5
1-1-7 Ext 17MHz Oscillator Circuit 5
1-1-8 SC Phase Shifter Circuit 5

1-1-1 Int 17MHz/14MHz Oscillator Circuit

Outline

This circuit oscillates the 17MHz/14MHz frequency in the internal sync mode and sends it to the sync generator IC. In the gen-lock/external sync mode, this circuit stops oscillating the 17MHz/14MHz frequency.

Details

When no signal is supplied to pin 37 of sync generator IC7, internal 17MHz oscillator consisting of crystal oscillator X2, CT2 (4.43MHz ADJ) and C41 oscillates 17MHz frequency. The oscillated 17MHz signal is sent to IC7, it is compared in phase with the signal oscillated by voltage controlled crystal oscillator (VCXO) consisting of X3, CT3 (FIELD DETECT), C44 and C45, and the phase difference is converted into the DC voltage.

The DC voltage corresponding to the phase difference is obtained at pin 46 of IC7 and sent to the VCXO to controlled the oscillating frequency by changing the capacitance of variable capacitance diode D3. The frequency-controlled signal is then fed to IC7 through pin 41 and it is compared with the 17MHz signal in phase. In this way, the phase lock loop (PLL) is made and pulses locked with the subcarrier signal are generated from IC7 respectively. When the PLL is stabilized, the VCXO oscillates approximately 14MHz. CT2 is a control for setting the subcarrier frequency by controlling the internally oscillated 17MHz frequency. CT3 is for setting lock range of VCXO.

1-1-2 Sync Generator Circuit

Outline

This circuit receives the 17MHz signal in internal sync mode or external sync mode and generates all sync signals used in the camera.

Details

The 4.43MHz subcarrier-1 (SC1) and subcarrier-2 (SC2) signals are obtained at pin 24 and 21 of sync generator IC7 and sent to the SC out circuit respectively.

The horizontal scanning start (Hs) pulse (A) at pin 11 of IC7 is sent through buffer IC4 (a) to differentiator consisting of C20 and R54 and it is differentiated ((B)). The negative portion of signal (B) is removed by D4 and the signal (C) is sent to control terminal (pin 10) of analog switch IC8(b). Pin 15 of IC8(b) is connected to pin 1 (+9V) during the positive portion of signal (C) and pin 15 is connected to pin 2 (ground) during the negative portion of signal (C). As a result, the clamp pulse (CP) (D) is made at pin 15 of IC8(b). The clamp pulse (CP) is then supplied through clamp pulse output Q13/Q14 and pin 14 of CN5 to other circuit.

The horizontal drive (HD) pulse (E) at pin 17 of IC7 is sent through buffer IC4(b), buffer IC9(c) and pin 12 of CN5 to other circuit.

The composite preblanking (pre BL) pulse (F) at pin 9 of IC7 is supplied to buffer IC4(c), buffer IC9(a) and pin 23 of CN5 to other circuit.

The composite blanking (BL) pulse (G) at pin 7 of IC7 is sent through buffer IC4(d), buffer IC9(b) and pin 25 of CN5 to other circuit.

The HD pulse (E) at pin 17 of IC7 is also sent through inverter IC3(a), horizontal scanning start (Hs) out Q11/Q12 and pin 17 of CN5 to other circuits as a Hs pulse.

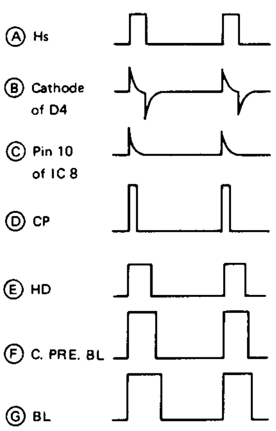


Fig. 1-1-2 Pulses

The sync signal which is used for M-format recorder (RECAM) and obtained at pin 16 of IC7 is sent via inverter IC3(b), buffer IC9(d) and pin 24 of CN5 to other circuits.

The burst flag pulse (BFP) at pin 13 of IC7 is supplied through inverter IC3(c), buffer IC9(e) and pin 20 of CN5 to other circuits.

The composite sync pulse at pin 14 of IC7 is fed through inverter IC3(d), buffer IC9(f), composite sync output Q5/Q8 and pin 22 of CN5 to other circuit.

The vertical scanning start (Vs) pulse at pin 18 of IC7 is supplied through inverter IC3(e), Vs out Q9/Q10 and pin 19 of CN5 to other circuits.

The vertical blanking (V BL) pulse at pin 3 of IC7 is supplied through inverter IC3(f) to control terminal (pin 11) of analog switch IC8(a). During positive portion of V BL signal, pin 14 of IC8(a) is connected to pin 13 (ground) and pin 14 is connected to pin 12 (+9V) during the negative portion of V BL signal. As a result, the positive VBL signal at pin 14 of IC8 (a) is fed through pin 21 of CN5 to other circuit.

1-1-3 SC1 Out Circuit

Outline

This circuit receives the subcarrier-1 (SC1) signal from the sync generator circuit and sends out to the other circuits.

Details

The SC1 signal is fed from the sync generator circuit through buffer Q1 to the band pass filter (BPF) CF1 whose center frequency is 4.43MHz. After harmonics of 4.43MHz is removed by the BPF, the SC1 signal is fed out through buffer Q2 and pins 3 and 28 of CN5 to other circuits.

1-1-4 SC2 Out Circuit

Outline

This circuit receives the subcarrier-2 (SC2) signal from the sync generator circuit and sends out to the other circuits.

Details

The SC2 signal whose phase is alternated every lines is fed from the sync generator circuit through inverter Q3/Q25 to the band pass filter (BPF) CF2 whose center frequency is 4.43MHz. After harmonics of 4.43MHz is removed by the BPF, the SC2 signal is fed out through buffer Q4 and pin 29 of CN5 to other circuits.

1-1-5 Sync Separation Circuit

Outline

This circuit receives the black burst signal or color signal supplied to the gen-lock input connector on the rear of camera or the gen-lock input connector on the remote control unit (RCU), and separates the sync and burst signal from the gen-lock signal. The separated sync and burst signal is fed to the sync generator circuit for the gen-lock/external sync mode.

Details

The gen-lock signal (the black burst or color signal) Ⓐ is sent through pin 13 of CN5 to base of Q15.

The base of sync separation Q23 receives gen-lock signal through buffer Q22 from pin 13 of CN5. The separated sync signal obtained at collector of Q23 is sent through amplifier Q24 and NOR gate (inverter) IC2(c) to pin 37 of IC7 in the sync generator circuit.

When it is fed to pin37 of IC7, the sync generator IC7 is converted into the gen-lock/external sync mode and pulses which are synchronized with the separated sync signal are generated.

If the sync signal is not applied to pin 37 of IC7, the sync generator IC7 remains in the internal sync mode. The separated sync signal Ⓑ obtained at the pin 10 of IC2(c) is also sent to breeze way pulse generator consisting of IC2(d), C55, R87, D2, Q6 and IC2(b).

The negative sync signal Ⓒ obtained at pin 13 of NOR gate (inverter) IC2 is sent through control-current-differential circuit consisting of C55 and R87, and D2 to base of switching Q6 and is changed to pulse Ⓔ

The negative breeze way gate pulse Ⓔ obtained at collector of switching Q6 is sent through NOR gate (inverter) IC2(b) to pin 3 of IC2(a) Ⓕ.

The gen-lock signal Ⓐ is also sent to burst gate consisting of Q15 and Q16. The positive blanking (BL) signal Ⓖ is sent to base of Q16 from sync generator IC7. The Q16 turns OFF during positive portion of BL signal and Q16 turns ON during negative portion of BL signal. As a result, sync and burst signal are detected. The detected signal Ⓗ is fed to 4.43MHz band pass filter consisting of L13 and C4 to remove the low frequency component and detect only burst signal Ⓘ. The detected burst signal is sent through amplifier consisting of Q17 to Q21 to pin 2 of NOR gate IC2(a). The NOR gate IC2 removes noise during the breeze way portion and detected burst signal obtained at pin 1 of IC2(a) is supplied to pin 35 of sync generator IC7. And the sync generator generates the subcarrier (SC) signal which is synchronized with the detected burst signa .

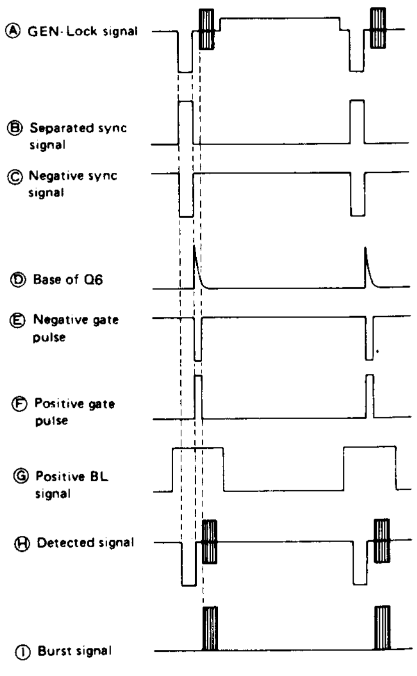


Fig. 1-1-5 Burst Signal

1-1-6 Gen-Lock 14MHz Oscillator Circuit

Outline

When the sync signal separated from the gen-lock signal is sent to the sync generator IC7, the H sync signal is compared with the horizontal drive (HD) pulse in phase in the sync generator IC7 and converted into the DC voltage which controls this circuit to oscillate the 14MHz frequency. It is sent to the sync generator IC7 to generate the HD pulse. In this way, the phase lock loop (PLL) circuit is made in the gen-lock/external sync mode and the 14MHz frequency is controlled to generate the HD pulse whose phase coincides with that of gen-lock sync signal. The sync generator IC7 is reset vertically in the IC7 by the sync signal supplied to the IC7.

Details

When the sync signal separated from the gen-lock signal in the sync separation circuit is sent to pin 37 of sync generator IC7, the HD pulse generated in IC7 and horizontal (H) sync signal separated from the sync signal are compared in phase in IC7. The phase difference is converted into the DC voltage and obtained at pin 45 of IC7. It is fed to the 14MHz voltage controlled oscillator (VCO) consisting of D1, C50 to C52, C49, L1, IC10(b) and CT4 (H.LOCK) and controls the oscillating frequency by changing the capacitance of variable capacitance diode D1. The pin 12 of IC10(b) receives gen-lock detect control from pin 38 of sync generator IC7. In the gen-lock/external sync mode, this potential is low level, and the VCO starts oscillating 14MHz.

The 14MHz frequency is fed back to pins 42 of IC7 through buffer IC10(a) to generate the HD pulse. In this way, the phase lock loop (PLL) circuit is made and the frequency of 14MHz VCO is controlled in order to generate the HD pulse whose relative phase matches that of H sync signal of gen-lock sync signal. CT4 (H.LOCK) is a control for setting the lock range of the PLL circuit. The relative phase between the HD pulse and the H gen-lock sync is adjusted by the DC voltage supplied to pin 1 of IC7. It is used to eliminate a horizontal phase difference between incoming gen-lock signal and internal oscillator. VR2 (H.PHASE) changes the DC voltage supplied to pin 1 of IC 7. VR(H.PHASE PRESET-1) and VR5(H.PHASE PRESET-2) set the adjusting range of VR2.

1-1-7 Ext. 17MHz Oscillator Circuit

Outline

In the gen-lock/external sync mode, this circuit oscillates the 14MHz to make the subcarrier (SC) signal whose frequency/phase is same as the burst signal of gen-lock signal.

Details

In the gen-lock/external sync mode, the SC signal generated in sync generator IC7 and the burst signal separated from the gen-lock signal and sent to pin 35 of IC7 are compared in phase in IC7. The phase difference in comparison is converted into the DC voltage and obtained at pin 36 of IC7 and it is sent to 14 MHz voltage controlled crystal osvillator (VCXO) consisting of crystal oscillator X1, D5, C56-C61 and CT1 (COLOR LOCK) to control the oscillating frequency by changing the capacitance of variable capacitance diode D5. The 14MHz frequency is fed back to pins 28 and 29 of IC7 to generate the SC signal. In this way, the phase lock loop (PLL) circuit is made and the frequency of VCXO is controlled in order to generate the SC signal whose frequency and relative phase matches that of gen-lock burst signal.

CT2 (COLOR LOCK) is a control for adjusting the lock range of the PLL circuit.

1-1-8 SC Phase Shifter Circuit

Outline

In the system using multiple cameras, the burst signal on each camera video signal should be adjusted to same phase. This circuit shifts the phase of subcarrier (SC) signal generated in the sync generator IC to adjust the phase of burst signal.

Details

SW1 (SC PHASE COARSE SWITCH) connected to pins 32 and 33 of sync generator IC7 shifts the phase of subcarrier signal from 0° to 360° in 90° step.

The SC signal (A) obtained at pin 22 of sync generator IC7 is sent to pin 22 of monostable multivibrator IC1(a). The output (B) of IC1(a) at pin 12 is fed to pin 2 of another monostable multivibrator IC1(b). The output (C) of IC1(b) at pin 13 is fed back to pin 25 of IC7. VR1 (SC PHASE) is a control to shift the subcarrier phase more than 90° by changing the power voltage for IC1 (a). By adjusting SW1 and VR1, the phase of subcarrier generated from IC7 can be shifted more than 360°.

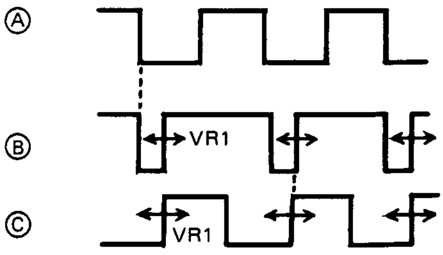


Fig. 1-1-8

1-2 Detail Board

The detail board contains the following circuits.

1-2-1 AGC Pulse Mix and White Clip Circuit 6
1-2-2 Carrier Oscillator and Modulation Circuit 7
1-2-3 1H Delay Signal Generator Circuit 7
1-2-4 2H Delay Signal Generator Circuit 7
1-2-5 V.Detail Signal Generator Circuit 7
1-2-6 H.Detail Signal Generator Circuit 8
1-2-7 Detail Out Circuit 9
1-2-8 G Signal Delay Circuit 9

1-2-1 AGC Pulse Mix and White Clip Circuit

Outline

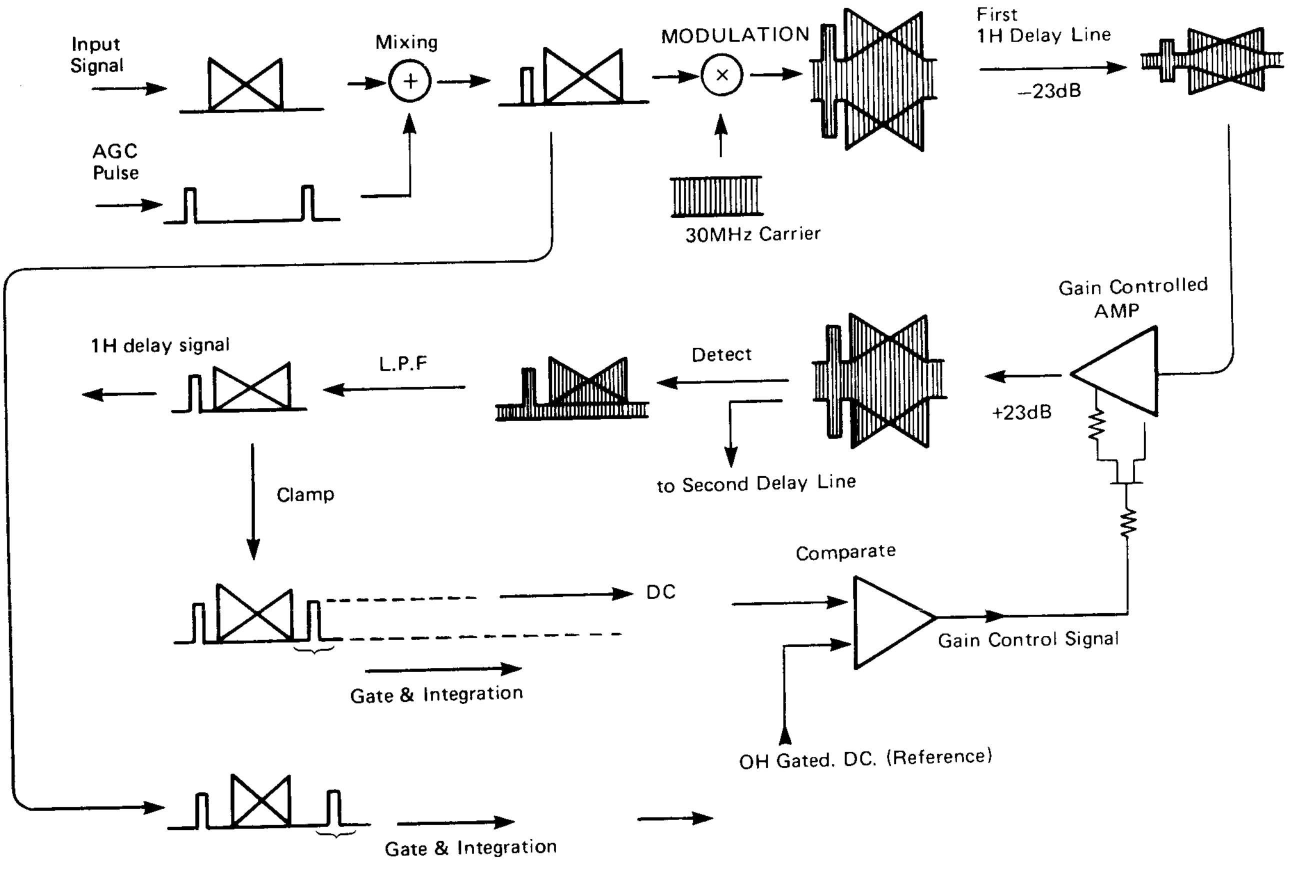
This circuit generates the AGC pulse from the horizontal drive (HD) pulse and it is mixed with the green (G) signal to maintain the vertical (V) detail (edge) balance by keeping levels constant among the non-delayed (0H), 1H (64 µs) delayed and 2H (128 µs) delayed G signal. This detail board employs a keyed AGC circuit. The principle of keyed AGC circuit is shown in Fig. 9-1.

The AGC pulse is mixed with non-delayed G signal as the reference signal. Then it is modulated by 30MHz carrier wave and delayed 1H (64 µs) period by 1H delay line DL2(a).

The 1H delayed G signal with AGC pulse is amplified by AGC amplifier IC2. The AGC pulse is detected by Q12 and the DC voltage corresponding to the 1H delayed AGC pulse level is fed to the comparator IC3(b).

On the other hand, non delayed (1H) AGC pulse is detected by Q42 and the DC voltage corresponding to the non-delayed AGC pulse level is also fed to the comparator IC3(b) as the reference voltage.

The output DC voltage of comparator IC3(b) corresponding to the level difference is fed to the gain controller Q7 and the 1H delayed G signal level is kept constant. The 2H delayed G signal level is also kept constant as in case of 1H delayed G signal to maintain the vertical detail signal balance.



Input Signal
Mixing
MODULATION
First 1H Delay Line
–23dB
AGC Pulse
30MHz Carrier
Gain Controlled AMP
1H delay signal
L.P.F
Detect
+23dB
to Second Delay Line
Clamp
Comparate
DC
Gain Control Signal
Gate & Integration
OH Gated. DC. (Reference)
Gate & Integration

Fig. 1-2-1 Principle of keyed AGC circuit

Details

The G signal from Process-1 board is mixed with the AGC pulse generated at the AGC pulse generator circuit at the base of Q13.

The G signal with AGC pulse obtained at the emitter of Q13 is clamped by Q14 and is supplied to the white clip circuit consisting of Q15 and Q16.

In the white clip circuit, the extremely high G signal is clipped since the 1H and 2H delay G signal circuits have limited dynamic range.

The white clipped G signal with AGC pulse is supplied to pin 4 of modulator IC1 through buffer Q17 and is also supplied to the vertical detail (edge) signal generator circuit.

1-2-2 Carrier Oscillator and Modulator Circuit

Outline

This circuit generates 30MHz carrier signal and modulates G signal by 30MHz carrier signal.

Details

The 30MHz carrier signal is generated by Q1 and crystal oscillator X 1 and is fed to pin 7 of modulator IC1. The G signal with AGC pulse is also fed from the emitter of Q17 to pin 4 of IC1.

The modulated G signal with AGC pulse obtained at pin 9 of IC1 is supplied to the 1H delay signal generator circuit.

1-2-3 1H Delay Signal Generator Circuit

Outline

This circuit receives the modulated G signal, delays 1H (63.5 μs) period and generates 1H delayed G signal.

Details

The modulated G signal from pin 9 of modulator IC1 is supplied 1H delay line DL2(a) through drive amp Q2, Q3, Q4, Q5 and Q6.

The modulated 1H delayed G signal is fed to pin 2 of AGC amp IC2 whose gain is controlled by the DC voltage supplied from pin 7 of AGC detector IC3(b) through Q7.

The amplified modulated 1H delayed G signal obtained at pin 6 (positive) and pin 7 (negative) of IC2 are fed to the bases of detector Q8 and Q9 respectively and converted into 1H delayed G signal.

The 1H delayed G signal obtained at the collectors of Q8 and Q9 is applied to the low pass filter consisting of L3, L4, C20, C21 and C85 to remove the 60MHz carrier component.

The 1H delayed G signal is supplied to G signal delay circuit, H and V.detail signal generator circuit and level dependent control circuit.

1-2-4 2H Delay Signal Generator Circuit

Outline

This circuit receives the modulated 1H delayed G signal, delays 1H period more (Total 2H) and generates 2H delayed G signal as in case of 1H delay signal generator circuit.

Details

The modulated 1H delayed G signal obtained at pin 7 of IC2 is fed to 1H delay line DL2(b) through drive amp Q19, Q20, Q21, Q22 and Q23 and is delayed 1H period more (Total 2H).

The modulated 2H delayed G signal is then amplified by AGC amp IC4 whose gain is controlled by the DC voltage supplied from pin 1 of AGC detector IC3(a) through Q24.

The amplified modulated 2H delayed G signal is fed to the detector Q25 and Q26 and 2H delayed G signal is obtained at the collectors of Q25 and Q26.

The 2H delayed G signal is then applied to the low pass filter consisting of L6, L7, C46, C47 and C86 to remove the 60MHz carrier component.

The 2H delayed G signal is supplied to the H and V. detail signal generator circuit.

1-2-5 V. Detail Signal Generator Circuit

Outline

This circuit generates V.detail signal by processing of non-delayed G signal (0H), 1H delayed G signal (1H) and 2H delayed G signal (2H) as;

V.Detail = ((0H) + (2H)) - (1H)

Details

The non-delayed G signal from the emitter of Q17 through buffer Q34 and 2H delayed G signal from the emitter of Q28 is mixed at the emitter of Q35.

The 1H delayed G signal from the emitter of Q10 through VR2 (V.BALANCE) is supplied to the base of Q35.

VR2 is a control for the V.detail signal balance.

VR1 (PULSE MIX) is a control for the blanking level of the V.detail signal to maintain the pedestal level same even if SW1 (DETAIL ON/OFF SWITCH) is switched ON/OFF.

The V.detail signal obtained at the collector of Q35 is fed to the low pass filter to remove the noise and harmonics of the V.detail signal.

The V.detail signal from the low pass filter is fed to the detail out circuit through VR3 (V.GAIN) and buffer Q36.

VR3 is a control for V.detail signal level.

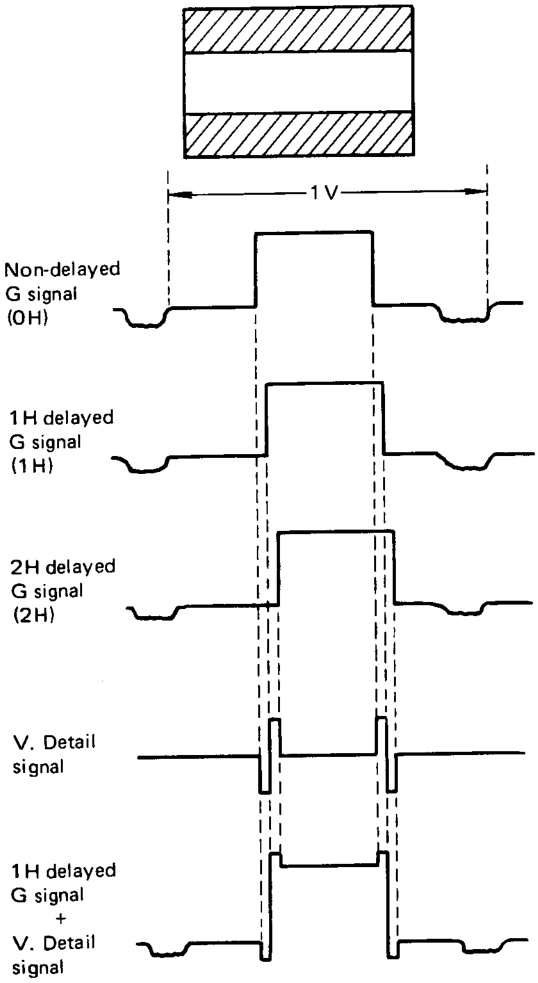


Fig. 1-2-5 V. Detail Signal Generator Circuit

1-2-6 H. Detail Signal Generator Circuit

Outline

This circuit generates H.detail signal to enhance the H resolution.

Details

The non-delayed G signal from the emitter of Q34, 1H delayed G signal from the emitter of Q10 and 2H delayed G signal from the emitter of Q28 are mixed at the base of Q37 to consist a comb filter.

The comb filter removes 4.43MHz and its harmonics to reduce the cross-color noise.

When the camera is aimed at an object (A) for example, the 1H delayed G signal (B) at the emitter of Q37 is fed to the emitter of Q49. The 1H delayed G signal (C) which is delayed 90ns by delay line L11 and obtained at the emitter of Q47 is applied to the base of Q49 through VR5 (H DETAIL BALANCE) and the 1H delayed (D) signal is made. The 1H and 90ns delayed G signal obtained at the emitter of Q47 is also forwarded to the delay line L12 and delayed again (180ns) (E) and is fed to the emitter of Q49 through Q48.

At the collector of Q49, the signal (B), (D) and (E) are mixed together in fixed proportion to make up the H.detail (aperture) signal (F).

The H.detail signal is mixed with the vertical (V) detail signal at the emitter of Q51 through VR4 (H DETAIL GAIN) and Q50. The H and V detail signal mixed is fed to the detail out circuit.

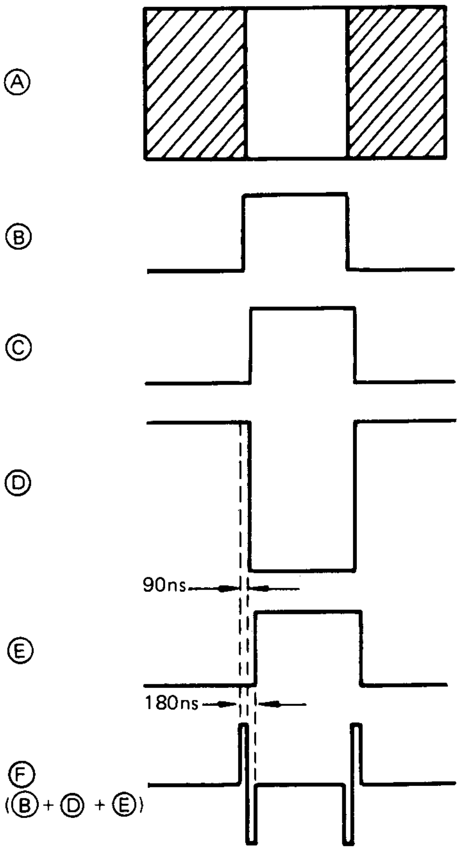


Fig. 1-2-6 H Detail Signal

1-2-7 Detail Out Circuit

Outline

This circuit receives the horizontal(H) and vertical(V) detail signal, mixes them and sends the mixed detail signal to the red (R), green (G) and blue (B) signal processing circuit in the Process-2 board. This circuit also reduces the noise on the detail signal and controls adding the detail signal to the R, G and B signal or not.

Details

The mixed detail signal amplified by Q51 is fed through buffer Q52 to clamp circuit Q53 where the blanking (BL) period of detail signal is clamped by the clamp pulse (CP) fed to the base of Q53 and the BL level becomes the emitter potential of Q53. The clamped detail signal is then supplied through buffer Q54 and amplifier IC5 to detail ON/OFF control circuit consisting of Q55. Q57 - Q59 connected to the base to Q56 is the detail signal dependent circuit.

The horizontal drive (HD) pulse is supplied to the base of Q55 and Q55 turns ON during positive period of HD pulse supplied to its base. Therefore the detail signal and noise during the BL period is removed. The detail control signal is also fed from pin 9 of CN6 to the base of Q55. In the detail OFF mode, the high potential is supplied to the base of Q55 and Q55 is turned ON. As a result, no detail signal is sent to Q56.

The 1H delayed G signal from the vertical detail signal circuit through buffer Q38 is clamped by Q39 and the BL period of G signal becomes the emitter potential of Q39. The potential at the emitter of Q58 is set by the DC voltage adjusted by VR6 (LEVEL DEPENDENT) and sent through buffer/temperature correction Q59. When the G signal (A) is sent to the base of Q58 for example, the detail signal (B) is sent to the base of Q56. At this time, Q58 is turned OFF during the G signal below the specified level and the gate potential of Q57 becomes +9V turning ON Q57. As a result, the detail signal corresponding to the G signal below specified level goes to the +9V line through C75 and Q57 and no detail signal is sent to Q56. Q58 is turned ON during the G signal above the specified level turning OFF Q57. Therefore, the detail signal is sent to the base of Q56. In this way, the detail signal corresponding to the low G signal is removed and the detail signal (C) is obtained at the emitter of Q56.

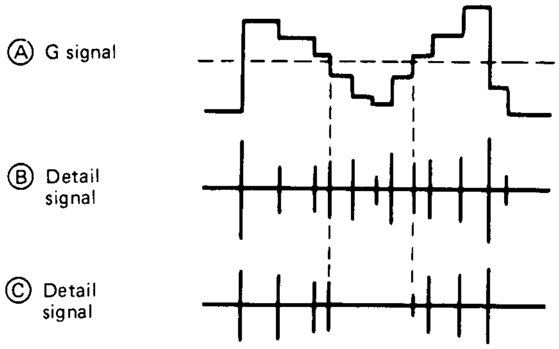


Fig. 1-2-7 Level Dependent

The detail signal is sent to the noise coring circuit which consists of D4 and D5. The detail signal (D) which includes the noise is fed to D4 and D5. The center (noise) portion of the detail signal is suppressed by threshold level of D4 and D5 (E). VR7 (NOISE SUPPRESS) adjusts the noise suppress level.

The detail signal whose level is set by VR8 (DETAIL GAIN) is sent through buffer Q61 and pin 28 of CN6 to the Process-2 board.

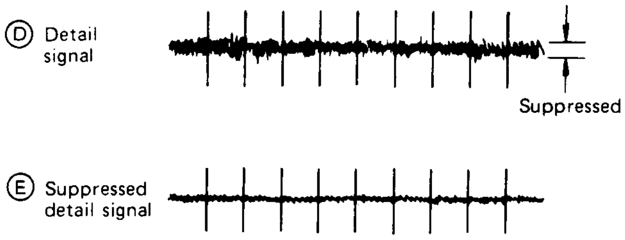


Fig. 1-2-8 Noise Suppression

1-2-8 G Signal Delay Circuit

Outline

The vertical (V) detail signal which is made from the green signal is delayed approximately 60ns from the G signal by the low pass filters used in the V.detail signal generator circuit. The horizontal (H) detail signal is also made from the 1H delayed G signal by the delay line used in the H datail generator circuit.

This circuit receives the 1H delayed G signal from the V.detail generator circuit, delays the 1H delayed G signal 150ns in order to match it with the detail signal in phase and sends it out to the Process-2 board.

Details

The 1H delayed G signal is sent from the V.detail generator circuit to delay line L10 where the 1H delayed G signal is delayed 150ns.

The delayed G signal is supplied through amplifier Q44, Q45 and Q46 to Process-2 board.

2. ADJUSTMENT PROCEDURE

o The comparison for adjustment procedure of WV-555B Series are described in the Table 2-1.

ADJUSTMENT PROCEDURE	WV-555	WV-555B
1. Test Equipment Required	A	A
2. Disassembling Procedure for Adjustment	A	A
2-1 Camera	A	A
2-2 1.5" Viewfinder WV-VF32	A	A
2-3 Camera Lens WV-LZ32/10	A	A
3. Pick-up Tube Replacement	A	A
3-1 Blue Pick-up Tube Replacement	A	A
3-2 Green Pick-up Tube Replacement	A	A
3-3 Red Pick-up Tube Replacement	A	A
4. Adjustment Procedure	A	A
4-1 Connection and Setting Up for Adjustment	A	A
4-2 Power Supply Adjustment	A	A
a) +9V adjustment (Mother board)	A	A
b) +5V adjustment (Mother board)	S2	S2
c) Pedestal preset adjustment (Mother board)	A	A
d) Battery warning adjustment (Mother board)	S4	S4
4-3 Sync Board Adjustment	A	A
a) 4.43 MHz adjustment	A	A
b) Field detect adjustment	A	A
c) Horizontal lock adjustment	S4	S4
d) Color lock adjustment	A	A
e) Horizontal phase adjustment	A	A or B
f) Confirmation of subcarrier phase adjustment	A	A
4-4 Encoder Board Adjustment	A	A
a) Color bar width adjustment	A	A
b) Carrier balance and white balance adjustment	A	A
c) Bar Pedestal, Y gain and Sync level adjustment	A	A
d) Chroma and Burst adjustment	A	A
e) REG balance adjustment	A	A
f) PIX output pedestal adjustment	A	A
4-5 Deflection and High Voltage AIC Board Adjustment	A	A
a) Target voltage adjustment	A	A
a') Rotation adjustment	S3	S3
b) Focus adjustment	A	B
c) Horizontal and Vertical size adjustment	A	A
d) Green beam current adjustment	A	A
e) Green beam alignment adjustment	A	A
f) Green centering adjustment	A	A
g) Green deflection coil rotation adjustment	A	A
h) Linearity adjustment	A	A
i) Red beam current adjustment	A	A
j) Red centering adjustment	A	A
k) Red beam alignment adjustment	S4	S4
l) Blue beam current adjustment	A	A
m) Blue centering adjustment	A	A
n) Blue beam alignment adjustment	S4	S4
o) Red registration adjustment	A	A
p) Blue registration adjustment	S4	S4
4-6 Preamplifier Board Adjustment	A	A
a) Frequency response adjustment	A	A

ADJUSTMENT PROCEDURE	WV-555	WV-555B
4-7 Process-1 Board Adjustment	A	A
a) Input gain adjustment	A	A
b) Dark shading adjustment	A	A
c) Blanking offset adjustment	A	A
4-8-1 Detail Board Adjustment (1H Vertical Enhancer Board)	A	–
a) Vertical detail (aperture) adjustment	A	–
b) Horizontal detail (aperture) adjustment	A	–
c) Detail (aperture) noise suppress adjustment	S3	–
d) Level dependent adjustment		
e) Detail gain adjustment	S3	–
4-8-2 Detail Board Adjustment (2H Vertical Enhancer Board)	–	B
a) Frequency response adjustment	–	B
b) V detail balance and V detail gain adjustment	–	B
c) H detail balance and H detail gain adjustment	–	B
d) Level dependent and noise suppress adjustment	–	B
e) Detail gain adjustment	–	B
f) Pulse mix adjustment	–	B
4-9 Process-2 Board Adjustment	A	A
a) G gamma, pedestal and gain adjustment	S3	S3
b) R gamma, pedestal and gain adjustment	A	A
c) B gamma, pedestal and gain adjustment	A	A
d) White balance fine adjustment	A	A
e) Camera pedestal adjustment	A	A
e') Confirmation of video signal adjustment	–	B
f) White clip adjustment	A	B
g) Feedback beam control adjustment	A	A
4-10 Auto Board Adjustment	A	A
a) Auto H. Subcentering adjustment	S4	S4
b) Gate pulse adjustment	A	A
c) Auto white control and Auto black control adjustment	A	A
d) Level indicator adjustment	A	A
e) AIC corner gate level adjustment	A	A
4-11 Automatic Iris Control Adjustment	A	A
a) AIC level adjustment	S4	S4
b) Lens AIC level adjustment	A	A
4-12 1.5" Viewfinder WV-VF32 adjustment	A	A
4-13 Camera Lens WV-LZ32/10 Adjustment	A	A

A : Original Service Manual for WV-555 (Order No. VKD83100784C8)
S2 : Supplement-2 Service Manual for WV-555 (Order No. VKD84110882S8)
S3 : Supplement-3 Service Manual for WV-555 (Order No. VKD84110883S8)
S4 : Supplement-4 Service Manual for WV-555 (Order No. VKD85030901S8)
B : Issued in this Service Manual for WV-555B

Table 2-1

2-1 Sync Board Adjustment

Note : The underline passages of (d) Horizontal phase adjustment on page 9 for 4-3 Sync Board Adjustment has been changed.

(d) Horizontal phase adjustment

Test points :	TP13 (GEN-LOCK)	Extension board
	TP22 (COMPOSITE SYNC)	Extension board
Adjust :	VR2 (H.PHASE)	Sync board
	VR4 (H.PHASE SUB1)	Sync board
	VR5 (H.PHASE SUB2)	Sync board

- Connect the Color Bar or Black Burst signal to the PIX OUT/GEN-LOCK IN connector of the camera.
- Set the monitor/PIX Select Switch to the Y position.
- Connect the oscilloscope to TP13 (G/L) and TP22 (C. SYNC) on the Extension board.
- Trigger the oscilloscope at H. rate. (Use TP8 (HD), Mother board).
- Adjust H.PHASE SUB1 VR4 so that the phase of sync signal at TP13 shifts 4.5 ± 0.2μsec when H. PHASE VR2 is turned fully clockwise and counter-clockwise.
- Turn H.PHASE VR2 fully clockwise and adjust H.PHASE SUB2 VR5 so that the sync of gen-lock signal at TP13 lags 4 μsec the sync signal at TP22.

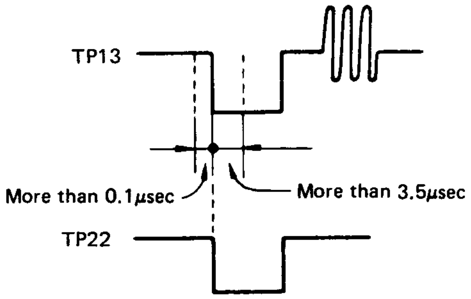


Fig. 4-3-1

- After confirming the above step, adjust VR2 so that the leading edges of both sync signals are coincident.

Steps denoted by shaded outlines do not have to be performed if only pick-up tubes are replaced.

2-2 Deflection and High Voltage AIC Board Adjustment

NOTE : The underline passages of (b) Focus adjustment on page 13 for 4-5 Deflection and High Voltage AIC Board Adjustment has been changed.

(b) Focus adjustment

Test points :	TP1 (G)	Process-1 board
	TP2 (R)	Process-1 board
	TP3 (B)	Process-1 board
	Collector of Q21	High voltage board
Adjust :	VR4 (R FOCUS)	High voltage board
	VR5 (G FOCUS)	High voltage board
	VR6 (B FOCUS)	High voltage board
	VR11 (DYNAMIC FOCUS)	High voltage board
	Backfocus adjusting screws	
Observe :	Monochrome underscanned video monitor	

- Set the flangeback adjusting ring on the lens to the standard position after loosening the flangeback lock knob. (Fig. 4-5-1)

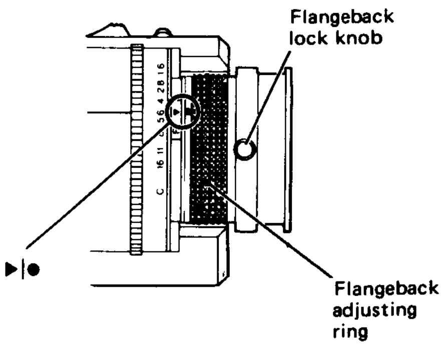


Fig. 4-5-1

- Turn DYNAMIC FOCUS VR11 fully clockwise.
- Set OVERSCAN SWITCH on the Deflection board to the NORMAL position.
- Connect the PIX/GEN-LOCK connector on the rear of camera to the monochrome underscanned video monitor.
- Set the Monitor/PIX Select Switch to the R-G position.
- Connect the capacitor 100μF 10V to TP2(R) on Process-2 board, (+ lead) and the ground. (- lead).

■ G focus adjustment

- Loosen the G coil lock screw (G LOCK) slightly. (Fig. 4-5-2)

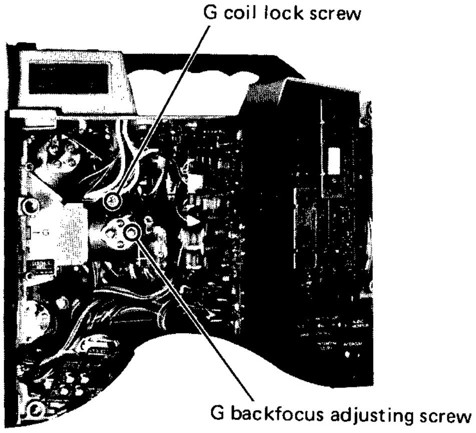


Fig. 4-5-2

- Set the lens iris to F1.4 in order to have minimum depth of focus (depth of field). If the picture on the monochrome video monitor is saturated, set the filter wheel on the side of camera to the position 2.
- Connect the oscilloscope to TP1(G) on the Process-1 board.
- Trigger the oscilloscope at H rate. (Use TP8(HD), Mother board)
- Aim the camera at the resolution chart or in-mega chart further than 2m from the camera.
- Zoom in (close up) and adjust the lens focus so that the modulation depth at the center of the picture becomes maximum.
- Zoom out (wide angle) and adjust the focus by turning the G backfocus adjusting screw (G BACKFOCUS) (Fig. 4-5-2).
- Zoom in again and adjust the lens focus. (Adjust G FOCUS VR5 on the High voltage board if the electrical focus is excessively out of focus.)
- Zoom out again and adjust the focus by turning the G backfocus adjusting screw.
- Repeat this procedure until the focus tracks throughout the zoom range.
- Reset the lens iris to F2.8 and the filter wheel to the position 1.
- Aim the camera at the resolution or in-mega chart so that the chart will fully occupies the screen of monitor.
- Adjust G FOCUS VR5 to obtain best focus at the center of picture. When the in-mega chart is used for the focus adjustment, the modulation depth at the center of in-mega signal becomes maximum at the best focus. (Fig. 4-5-3)

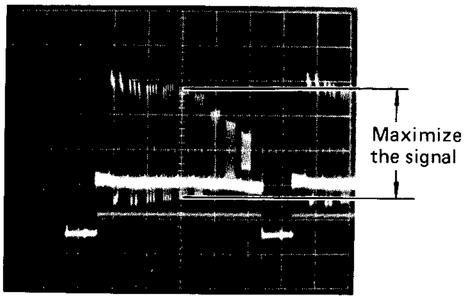


Fig. 4-5-3

- Connect the oscilloscope to collector of Q21 on the High voltage board.
- Trigger the oscilloscope at H rate. (Use TP8 (HD), Mother board.)
- Turn DYNAMIC FOCUS VR11 back slowly and stop at a point where the H parabola signal just appears completely. (Fig. 4-5-3')

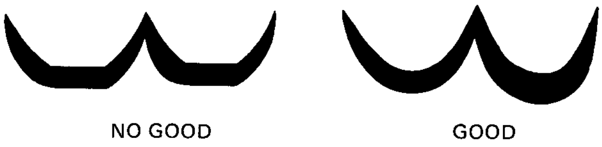


Fig. 4-5-3'

■ R focus adjustment

- Connect the capacitor 100μF 10V to TP1(G) on Process-2 board (+ lead) and the ground (- lead).
- Connect the Monitor/PIX Select Switch to R-G position.
- Connect PIX/GEN-LOCK connector to the monochrome underscanned monitor.
- Connect the oscilloscope to TP2(R) on the Process-1 board.
- Trigger the oscilloscope at H rate. (Use TP8(HD), Mother board.)
- Set the filter wheel on the side of camera to the position 2 and the lens iris to F1.4 in order to have minimum depth of focus.
- Aim the camera at the resolution chart or in-mega chart.

- Zoom in (close up) while observing the monochrome underscanned video monitor.
- Loosen the R coil lock screw (R LOCK) slightly. (Fig. 4-5-4)

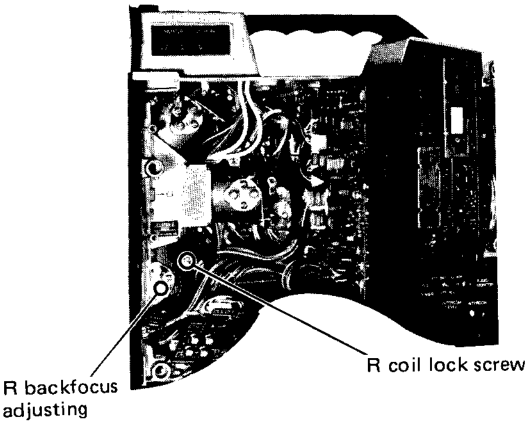


Fig. 4-5-4

- Adjust the focus by turning the R backfocus adjusting screw (R BACKFOCUS) (Fig. 4-5-4) while observing the oscilloscope.

  Note: Do not adjust the lens focus when adjusting the R backfocus.

- Reset the filter wheel to the position 1 and the lens iris to F2.8.
- Adjust R FOCUS VR4 to obtain best focus at the center of picture. When the in-mega chart is used for the focus adjustment, the modulation depth at the center of in-mega signal becomes maximum at the best focus. (Fig. 4-5-3)
- Repeat adjusting the R backfocus adjusting screw and R FOCUS VR4 to obtain best focus.
- Tighten the R coil lock screw (R LOCK) and make sure that the focus remains properly adjusted.

■ **B focus adjustment**

- Connect PIX/GEN-LOCK connector to the monochrome underscanned monitor.
- Set the Monitor/PIX Select Switch to B-G position.
- Connect the capacitor 100μF 10V to TP1(G) on Process-2 board (+ lead) and ground (- lead).
- Connect the oscilloscope to TP3 (B) on the Process-1 board.
- Trigger the oscilloscope at H rate. (Use TP8(HD), Mother board.)
- Set the filter wheel on the side of camera to the position 2 and the lens iris to F1.4 in order to have minimum depth of focus.
- Aim the camera at the resolution chart or in mega chart.
- Zoom in (close up) while observing the monochrome underscanned video monitor.
- Loosen the B coil lock screw (B.LOCK) slightly. (Fig. 4-5-5)

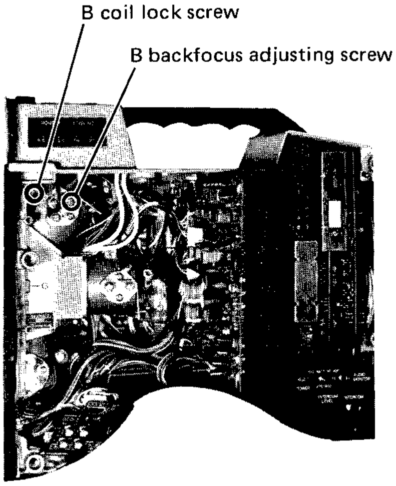


Fig. 4-5-5

- Adjust the focus by turning the B backfocus adjusting screw (B BACKFOCUS) while observing the oscilloscope. (Fig. 4-5-5)

  Note : Do not adjust the lens focus when adjusting the B backfocus.

- Reset the filter wheel to the position 1 and the lens iris to F2.8.
- Adjust B FOCUS VR6 to obtain best focus at the center of picture. When the in-mega chart is used for the focus adjustment, the modulation depth at the center of in mega signal becomes maximum at the best focus. (Fig. 4-5-3)
- Repeat adjusting the backfocus adjusting screw and B FOCUS VR6 to obtain best focus.
- Tighten the B coil lock screw (B LOCK) and make sure that the focus remains properly adjusted.

2-3 Detail Board Adjustment

NOTE : 4-8 Detail Board Adjustment on page 26 has been changed.

o Set the Monitor/PIX Select Switch to the Y position.

Steps denoted by shaded outlines do not have to be performed if only pick-up tubes are replaced.

(a) Frequency response adjustment

Test points :	TP1 (1H)	Detail board
	TP3 (0H)	Detail board
Adjust :	CT1 (FREQ. RESPONSE)	Detail board

- Aim the camera at the in-mega chart and set the lens iris to F2.8.
- Connect the oscilloscope to TP1 (1H) and TP3 (0H) on the Detail board.
- Trigger the oscilloscope at H rate. (Use TP8 (HD), Mother board.)
- Overlay the 1H-delayed signal and non-delayed signal on the oscilloscope.
- Adjust FREQ. RESPONSE CT1 on the Detail board so that the frequency response at TP1 and TP3 is equal. (The envelop of in-mega signal at TP1 and TP3 becomes equal.)

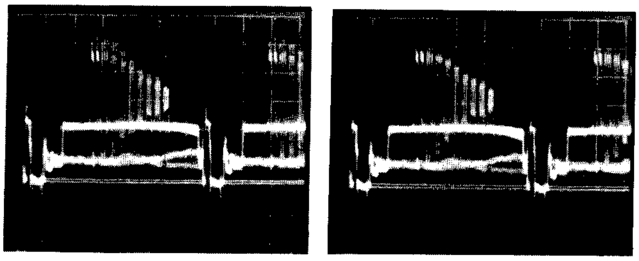

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Fig. 4-8-1

(b) V detail balance and V detail gain adjustment

Test points :	TP4	Process-2 board
	TP4 (V.DETAIL)	Detail board
Adjusts :	VR2 (V.BALANCE)	Detail board
	VR3 (V.GAIN)	Detail board

- Aim the camera at the window chart.

o Connect the oscilloscope to TP4 on the Process-2 board and trigger the oscilloscope at H rate. (Use TP8 (HD), Mother board.)

o Adjust the lens iris so that the G signal at TP4 on the Process-2 board becomes 1.6Vp-p.

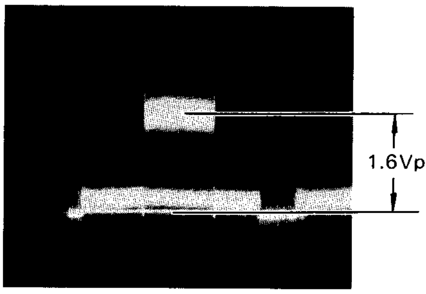


Fig. 4-8-2

- Connect the oscilloscope to TP4 (V.DETAIL) on the Detail board.
- Adjust the V DETAIL BALANCE VR2 to cancel the video signal and V edge signal is obtained.
- Trigger the oscilloscope at V rate. (Use TP7 (VD), Mother board.)
- Adjust V DETAIL GAIN VR3 so that the left side of the V edge signal becomes 200mVp-p.

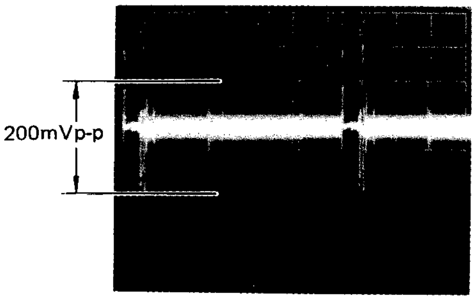


Fig. 4-8-3

(c) H detail balance and H detail gain adjustment

Test points :	TP6 (H.DETAIL)	Detail board
	TP4 (G)	Process-2 board
Adjusts :	VR4 (H.GAIN)	Detail board
	VR5 (H.BALANCE)	Detail board

- Aim the camera at the window chart so that the chart fully occupies the raster.
- Connect the oscilloscope to TP4(G) on the Process-2 board and trigger the oscilloscope at H rate. (Use TP8 (HD), Mother board.)
- Adjust the lens iris so that the G signal at TP4 on the Process-2 board becomes 1.6Vp-p.
- Connect the oscilloscope to TP6 (H.DETAIL) on the Detail board and trigger the oscilloscope at H rate.
- Adjust H BALANCE VR5 to cancel the video signal.
- Adjust H GAIN VR4 so that the H detail (edge) signal at TP6 becomes 100mVp-p.

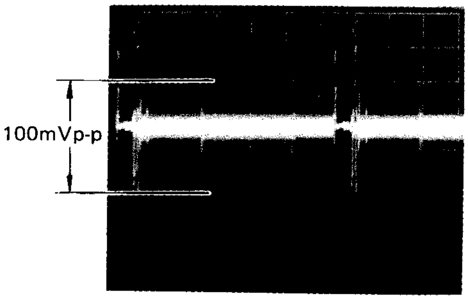


Fig. 4-8-4

Steps denoted by shaded outlines do not have to be performed if only pick-up tubes are replaced.

(d) Level dependent and noise suppress adjustment

Test points :	VIDEO OUT	
	TP7 (DETAIL OUT)	Detail board
Adjusts :	VR6 (LEVEL DEPENDENT)	Detail board
	VR7 (NOISE SUPPRESS)	Detail board

- Turn LEVEL DEPENDENT VR6 and NOISE SUPPRESS VR7 fully clockwise.
- Aim the camera at the logarithmic gray scale chart.
- Observe the waveform monitor or connect the oscilloscope to terminated VIDEO OUT signal.
- Trigger the oscilloscope at H rate. (Use TP8 (HD), Mother board.)
- Adjust the lens iris so that the black chip of the gray scale signal at VIDEO OUT becomes 84mVp-p from the blanking level.

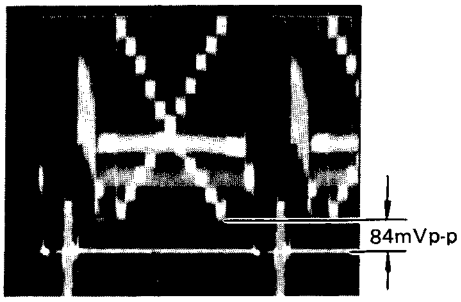


Fig. 4-8-5

- Adjust LEVEL DEPENDENT VR6 so that the noise on the black chip (zero step) of the gray scale waveform starts being suppressed.

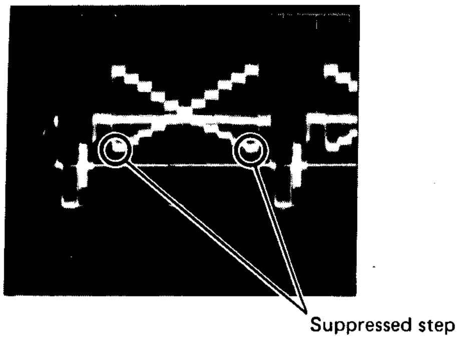


Fig. 4-8-6

- Connect the oscilloscope to TP7 (DETAIL OUT) on the Detail board.
- Trigger the oscilloscope at H rate. (Use TP8 (HD), Mother board.)
- Note the noise level of the detail signal as A mVp-p.

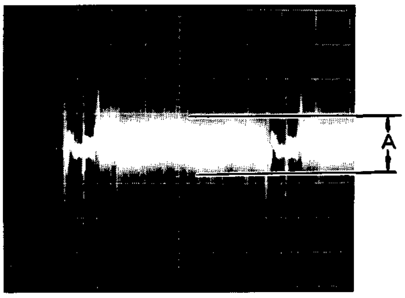


Fig. 4-8-7

- Adjust the NOISE SUPPRESS VR7 on the Detail board so that the noise level becomes 1/4 AmVp-p.

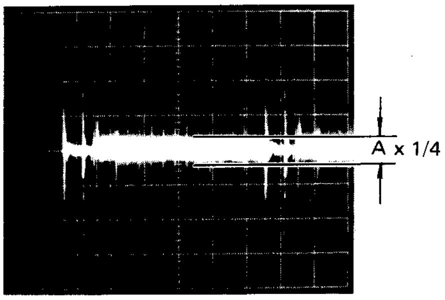


Fig. 4-8-8

(e) Detail gain adjustment

Test point :	VIDEO OUT	
Adjusts :	VR8 (DETAIL GAIN)	Detail board
	VR4 (H GAIN)	Detail board
	VR6 (LEVEL DEPENDENT)	Detail board

- Aim the camera at the window chart so that the chart fully occupies the raster.
- Set the Monitor/PIX Select Switch to the Y position and set the DETAIL ON/OFF Switch on the Detail board to ON position.
- Observe the waveform monitor or connect the oscilloscope to terminated VIDEO OUT signal.
- Trigger the oscilloscope at V rate. (Use TP7 (VD), Mother board.)
- Set the lens iris so that the white level of the white set chart signal becomes 500mVp-p from the black level of the window chart signal and note this level as A.

- Adjust the DETAIL GAIN VR8 on the Detail board so that the vertical detail (aperture) signal B becomes B/A x 100 = 125 5% from the black level of the window chart signal.

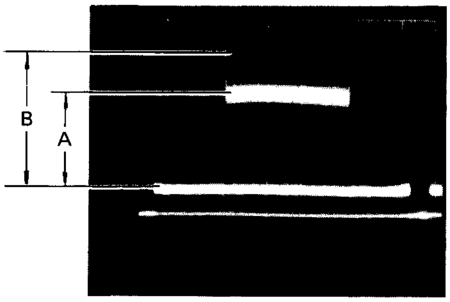


Fig. 4-8-9

- Trigger the oscilloscope at H rate. (Use TP8 (HD), Mother board.).
- Confirm that the horizontal detail (aperture) signal B and C is (B+C)/2A x 100 = 115 ±5%. If not, readjust the H GAIN VR4 on the Detail board.

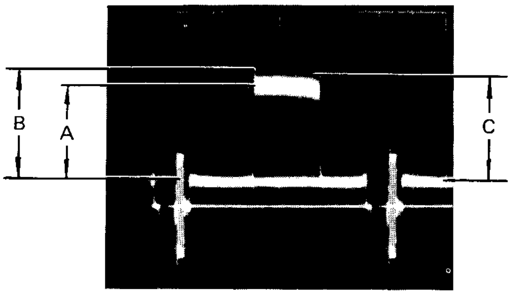


Fig. 4-8-10

- Set the lens iris so that the white level of the white set chart signal becomes 178mVp-p from the black level of the window chart signal and note this level as A.
- Trigger the oscilloscope at V rate. (Use TP7 (VD), Mother board.)
- Confirm that the vertical detail (aperture) signal B is B/A x 100 = 115% or higher. If not, readjust LEVEL DEPENDENT VR6 on the Detail board.

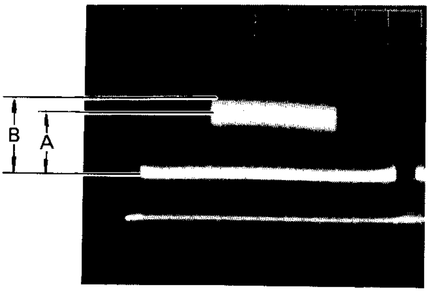


Fig. 4-8-11

Steps denoted by shaded outlines do not have to be performed if only pick-up tubes are replaced.

(f) Pulse mix adjustment

Test point :	TP4 (G)	Process-2 board
Adjust :	VR1 (PULSE MIX)	Detail board

- Cap on the lens or set the filter wheel to the position 4.
- Connect the oscilloscope to TP4 (G) and trigger the oscilloscope at H rate (Use TP8 (HD), Mother board).
- Adjust the G PEDESTAL VR4 on the Process-2 board so that the G pedestal level becomes approximately 0.2V from the blanking level as shown in Fig. 2-2-16.
- Set the DETAIL ON/OFF Switch SW1 on the Detail board to OFF position and note the pedestal level at TP4.
- Set the DETAIL ON/OFF Switch SW1 to ON position and adjust PULSE MIX VR1 on the Detail board so that the pedestal level at TP4 is the same as the noted level. (Fig. 4-8-12)

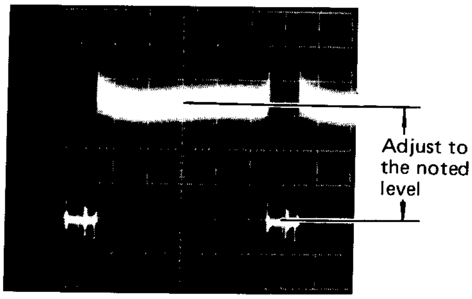


Fig. 4-8-12

- Set the DETAIL ON/OFF Switch SW1 to OFF position and note the pedestal level again.
- Set the DETAIL ON/OFF Switch SW1 to ON position and adjust VR1 so that the pedestal level is the same as the noted level.
- Repeat this procedure until the pedestal level stays the same by operating the DETAIL ON/OFF Switch SW1 ON and OFF.

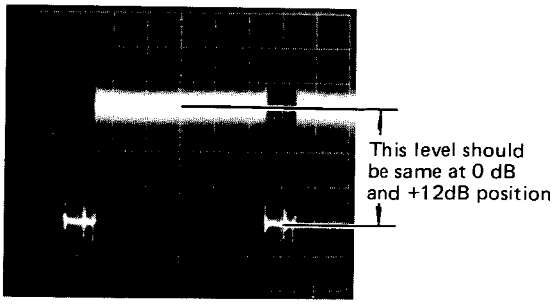


Fig. 4-8-13

- Set the DETAIL ON/OFF Switch SW1 to ON position.

2-3 Process-2 Board Adjustment

NOTE : The underline passages of (e) Camera pedestal adjustment on page 31 for 4-9 Process-2 Board Adjustment has been changed.

(e) Camera pedestal adjustment

Test point :	VIDEO OUT	
Adjust :	VR12 (CAMERA PEDESTAL)	Encoder board

- Cap on the lens or set the filter wheel to the position 4.
- Connect the oscilloscope to the terminated VIDEO OUT signal or connect the VIDEO OUT to the waveform monitor.
- Trigger the oscilloscope at H rate. (Use TP8(HD), Mother board.)
- Adjust CAMERA PEDESTAL VR12 so that the camera pedestal level is 35mVp-p. (Fig. 4-9-13)

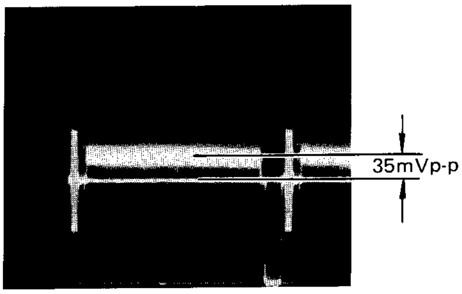


Fig. 4-9-13

(e') Confirmation of video out signal

NOTE : Adjustment procedures of Confirmation of video out signal between (e) Camera pedestal adjustment and (f) White clip adjustment for 4-9 Process-2 Board Adjustment has been added.

Test point :	VIDEO OUT	
Adjusts :	VR1 (B PEDESTAL)	Process-2 board
	VR2 (B GAMMA)	Process-2 board
	VR3 (B GAIN)	Process-2 board
	VR4 (G PEDESTAL)	Process-2 board
	VR5(G GAMMA)	Process-2 board
	VR6 (G GAIN)	Process-2 board
	VR7 (R PEDESTAL)	Process-2 board
	VR8 (R GAMMA)	Process-2 board
	VR9 (R GAIN)	Process-2 board

- Aim the camera at the gray scale chart and set the lens iris to F2.8.
- Connect the oscilloscope to the terminated VIDEO OUT signal or connect the VIDEO OUT to the waveform monitor.
- Trigger the oscilloscope at H rate. (Use TP8 (HD), Mother board.)
- Confirm that the top step of gray scale waveform is 0.7Vp-p, the black step (lowest step) of gray scale waveform is 0.084Vp-p and the 5th step (crossing step) of gray scale waveform is 0.413Vp-p.

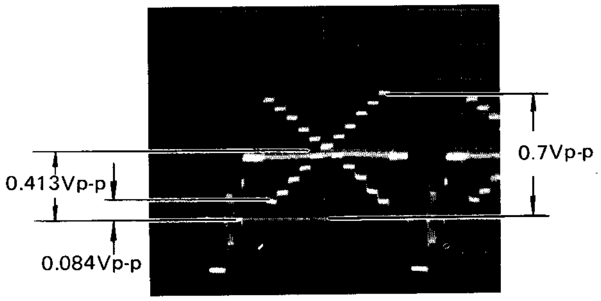


Fig. 4-9-13-1

- If not, readjust G PEDESTAL VR4, G GAMMA VR5 and G GAIN VR6 on the Process-2 board and then readjust B PEDESTAL VR1, B GAMMA VR2, B GAIN VR3, R PEDESTAL VR7, B GAMMA VR8 and R GAIN VR9 on the Process-2 board so that the carrier on the PAL signal is minimum.

3. LOCATION OF TESTPOINTS AND ADJUSTING CONTROLS

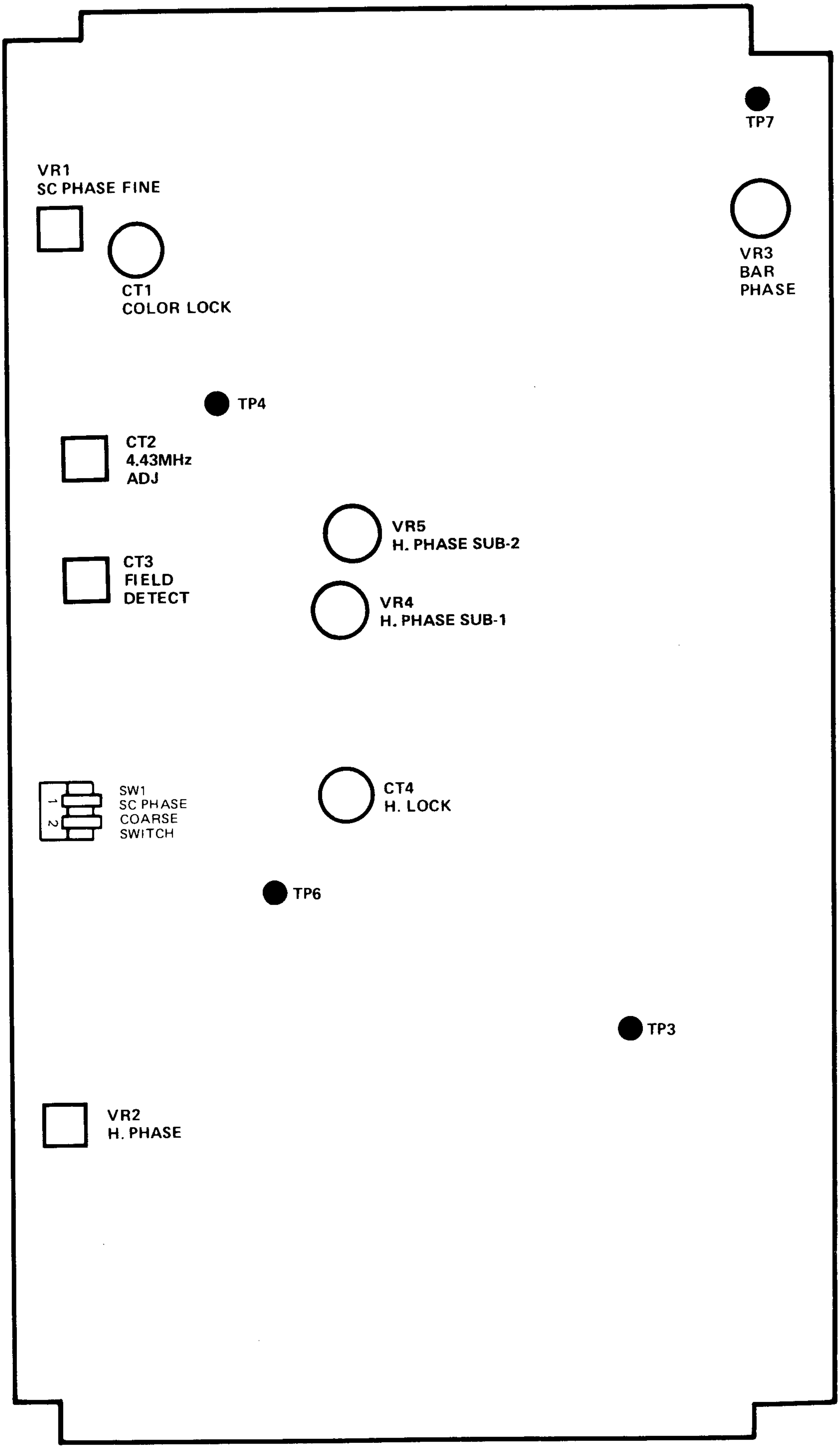
o The comparison for location of test points and adjustment control of WV-555B Series are described in the Table 3-1.

LOCATION OF TEST POINTS AND ADJUSTMENT CONTROLS	WV-555	WV-555B
1. Mother Board	A	A
2. Sync Board	A	A or B
3. Encoder Board	A	A
4. Deflection Board	A	A
5. High Voltage AIC Board	A	A
6. Process-1 Board	A	A
7. Detail Board	A	B
8. Process-2 Board	A	A
9. Auto Board	A or S4	S4
10. 1.5" Viewfinder WV-VF32	A	A

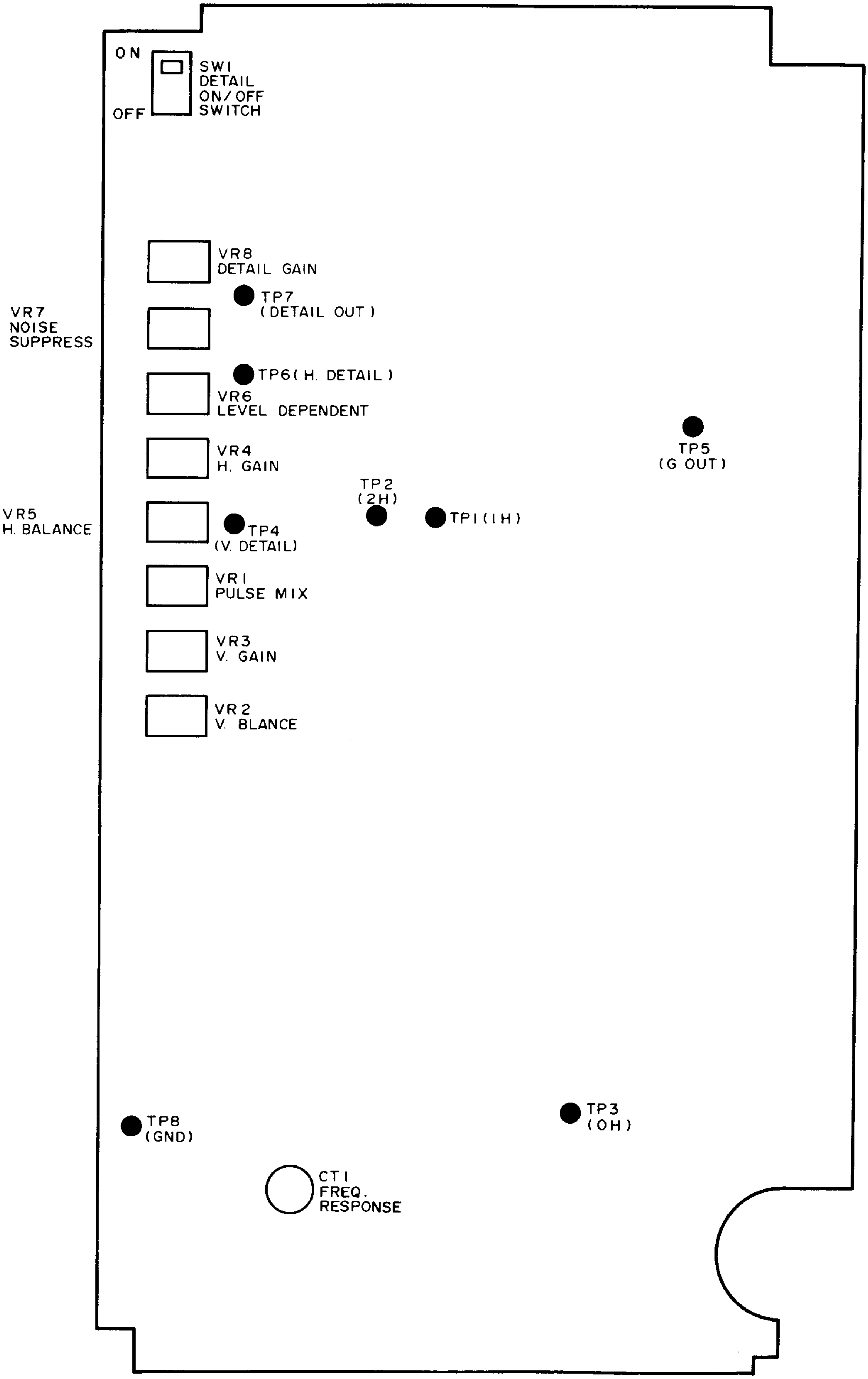
A : Original Service Manual for WV-555 (Order No. VKD83100784C8)
S1 : Supplement-1 Service Manual for WV-555 (Order No. VKD84060842S8)
S4 : Supplement-4 Service Manual for WV-555 (Order No. VKD85030901S8)
B : Issued in this Service Manual for WV-555B

Table 3-1

SYNC BOARD — Component Side —


TP7
VR1
SC PHASE FINE
CT1
COLOR LOCK
VR3
BAR
PHASE
TP4
CT2
4.43MHz
ADJ
VR5
H. PHASE SUB-2
CT3
FIELD
DETECT
VR4
H. PHASE SUB-1
1
2
SW1
SC PHASE
COARSE
SWITCH
CT4
H. LOCK
TP6
TP3
VR2
H. PHASE

DETAIL BOARD —Component Side —


ON
OFF
SW1
DETAIL
ON/OFF
SWITCH
VR8
DETAIL GAIN
TP7
(DETAIL OUT)
VR7
NOISE
SUPPRESS
TP6(H. DETAIL)
VR6
LEVEL DEPENDENT
VR4
H. GAIN
TP5
(G OUT)
TP2
(2H)
VR5
H. BALANCE
TP4
(V. DETAIL)
TP1(1H)
VR1
PULSE MIX
VR3
V. GAIN
VR2
V. BLANCE
TP8
(GND)
TP3
(OH)
CT1
FREQ.
RESPONSE

4. BLOCK DIAGRAM, SCHEMATIC DIAGRAM and CONDUCTOR VIEW

o The comparison for block diagram of WV-555B Series is described in the Table 4-1.

BLOCK DIAGRAM	WV-555	WV-555B
1. Process-1 Board	A	A
2. Process-2 Board	A	A
3. Encoder Board	A	A
4. Auto Board	A	A
5. Sync Board	A	A or B
6. Deflection Board	A	A
7. High Voltage AIC Board	A	A
8. Detail Board	A	B
9. 1.5" Viewfinder WV-VF32	A	A

Table 4-1

o The comparison for schematic diagram and conductor view of WV-555B Series are described in the Table 4-2.

SCHEMATIC DIAGRAM and CONDUCTOR VIEW	WV-555	WV 555B
1. Pre-Preamplifier and Preamplifier Board	A	A
2. Process-1 Board	A, S4	A, S4
3. Process-2 Board	A, S4	A, S4, B
4. Encoder Board	A, S3, S4	A, S3, S4
5. Auto Board	A or S1	S1, S3, B
6. Sync Board	A	A, S3 or B
7. Deflection Board	A	A, B
8. High Voltage AIC Board	A, S3	A, S3, B
9. Detail Board	A	B
10. Mother Board	A, S3	A, S3, B
11. 1.5" Viewfinder WV-VF32	A	A
12. Mic Board	A, S3	A, S3
13. Centering and ACC-MAN Select Board	A	A
14. Lens Control Board WV-LZ32/10	A	A
15. Battery Charger WV-BC32	A	A
WIRING DIAGRAM	A	A

A : Original Service Manual for WV-555 (Order No. VKD83100784C8)
S1 : Supplement-1 Service Manual for WV-555 (Order No. VKD84060842S8)
S3 : Supplement-3 Service Manual for WV-555 (Order No. VKD84110883S8)
S4 : Supplement-4 Service Manual for WV-555 (Order No. VKD85030901S8)
B : Issued in this Service Manual for WV-555B

Table 4-2

o The SCHEMATIC DIAGRAM and CONDUCTOR VIEW have been changed to improve for the Process-2 Board, Auto Board, Deflection board, High Voltage AIC Board, Detail Board, Sync Board and Mother Board.

Mother Board

o C22 on the Mother board has been changed to prevent the ringing of +9V power line from serial No. 52A00001 and higher.

Process-2 Board

o The Blue and Red output DC level on the Process-1 board are different between WV-555B and WV-N3. Therefore, the input capacitor C9 and C16 on the Process-2 board have been changed to nonpolarized electrolytic capacitor for standardization of WV-555B and WV-N3 from serial No. 51A00001 and higher.

o C43, C44 and C45 on the Process-2 board have been added in the signal processing circuit to improve the signal to noise ratio from serial No. 54A00001 and higher.

Auto Board

o The microprocessor IC14, R6 and R16 on the Auto board have been changed to improve the accuracy of the Auto Centering function from serial No. 49A00001 and higher.

Deflection Board

o The alignment circuit on the Deflection board has been changed to prevent the oscillation of the alignment circuit from serial No. 49A00001 and higher.

o R40 on the Deflection board has been changed to increase the horizontal deflection signal from serial No. 4YA00001 and higher.

High Voltage Board

o R61 and R62 on the High voltage board have been changed to prevent the chroma beat of corner picture from serial No. 4XA00001 and higher.

Detail Board

o R151 on the Detail board has been changed to improve the noise suppress when the high gain switch is set to +9 dB or +18 dB position from serial No. 52A00001 and higher.

o The amplifier circuit has been added in the detail out circuit to increase the detail signal level from serial No. 49A00001 and higher.

Sync Board

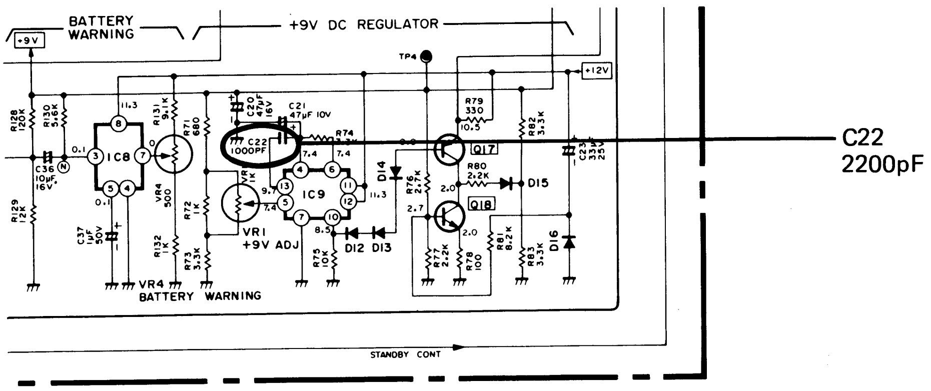
o VR4 and VR5 on the Sync board have been added to expand the variable range of H. PHASE from serial No. 49A00001 and higher.

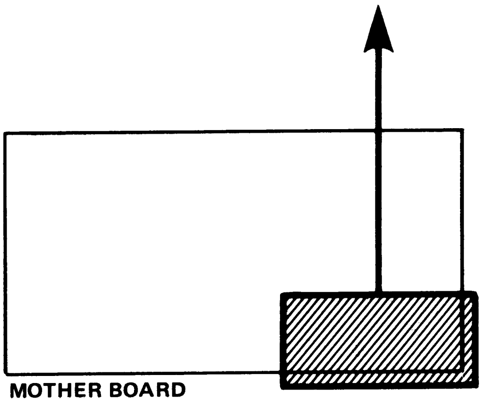
o R21 and C36 on the Sync board have been changed to improve stability of sync separation when the unit is warmed up from serial No. 51A00001 and higher.

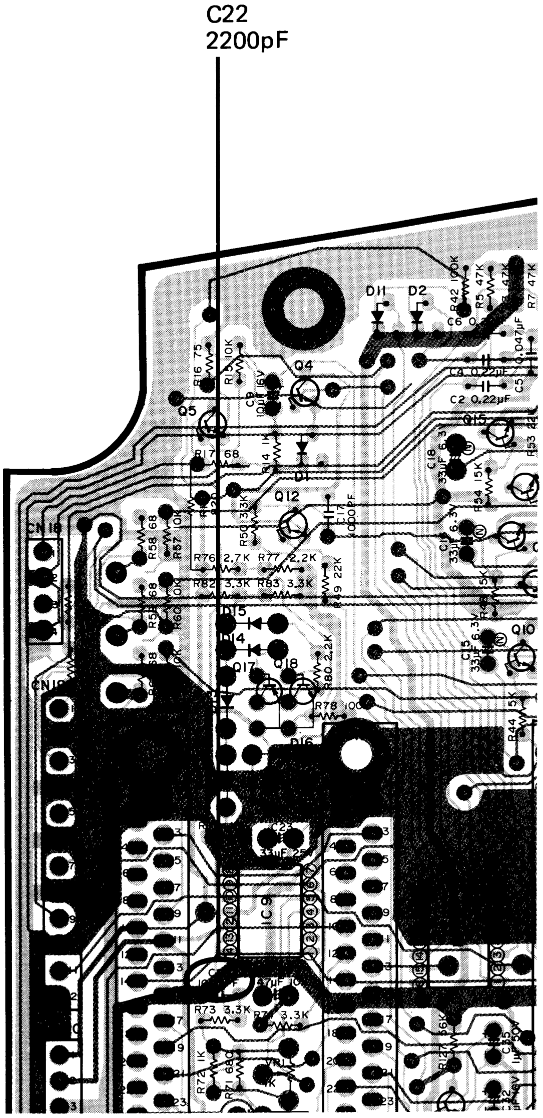
Exploded View of Camera (WV-555)

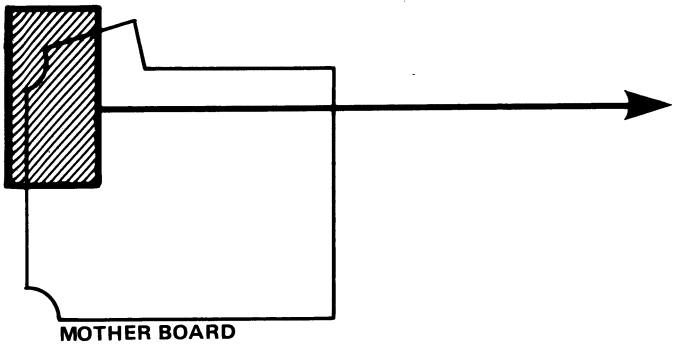
o M150 (Spacer) on the Camera chassis has been added to improve the RF interference from serial No. 48A00001 and higher.

4-1 Mother Board

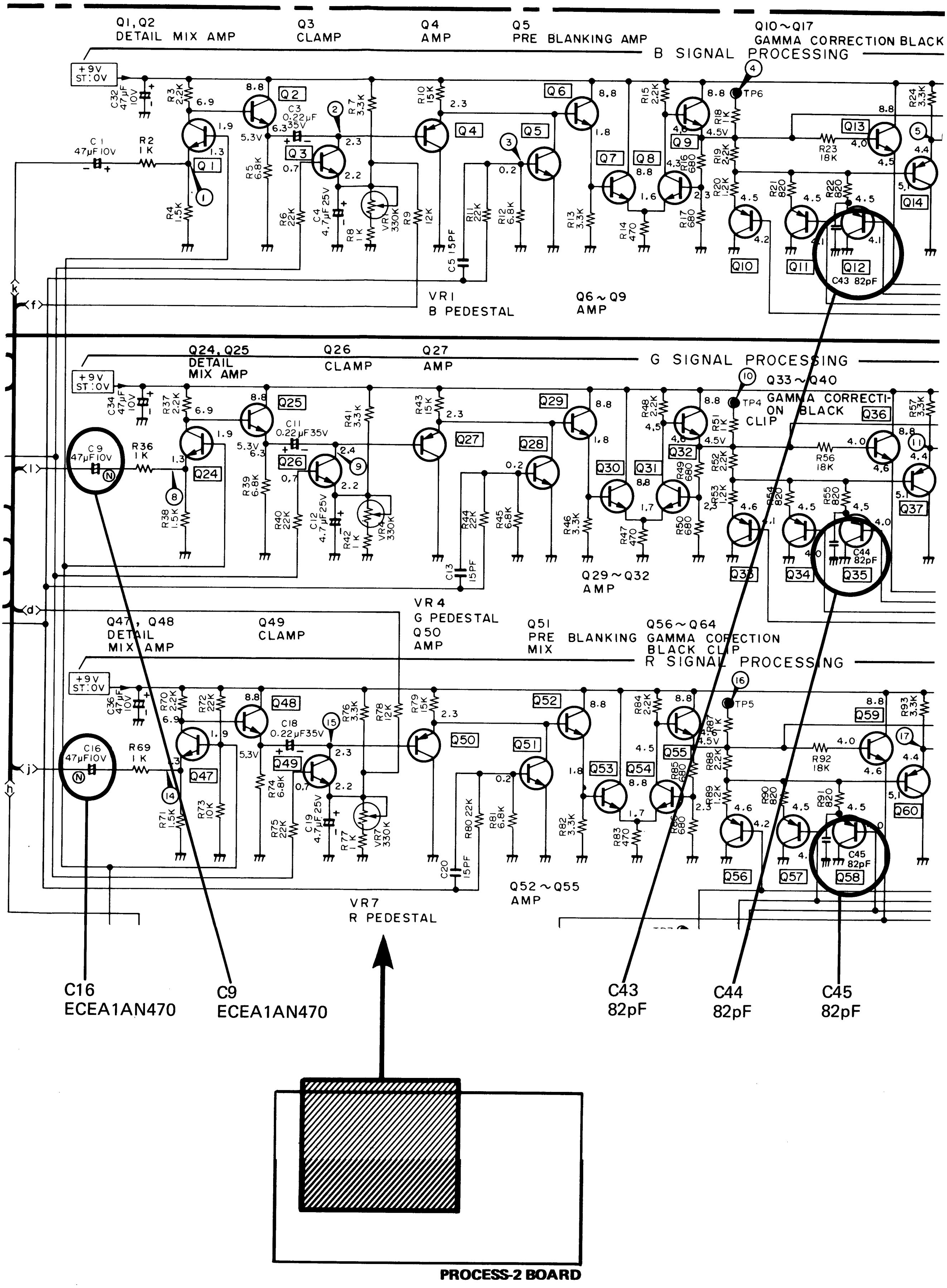

BATTERY WARNING
+9V DC REGULATOR
+9V
+12V
TP4
R128 120K
R130 5.6K
R129 12K
C36 10µF 16V
N
IC8
R131 9.1K
R71 680
VR4 500
R132 1K
C37 1µF 50V
R72 1K
R73 3.3K
VR4 BATTERY WARNING
C20 47µF 16V
C21 47µF 10V
C22 1000PF
R74 3.3K
VR1 1K
VR1 +9V ADJ
IC9
R75 10K
D12 D13
D14
R76 2.7K
R77 2.2K
R78 100
R79 330
Q17
Q18
R80 2.2K
D15
R81 8.2K
R82 3.3K
R83 3.3K
C23 33µF 25V
D16
STANDBY CONT
C22
2200pF

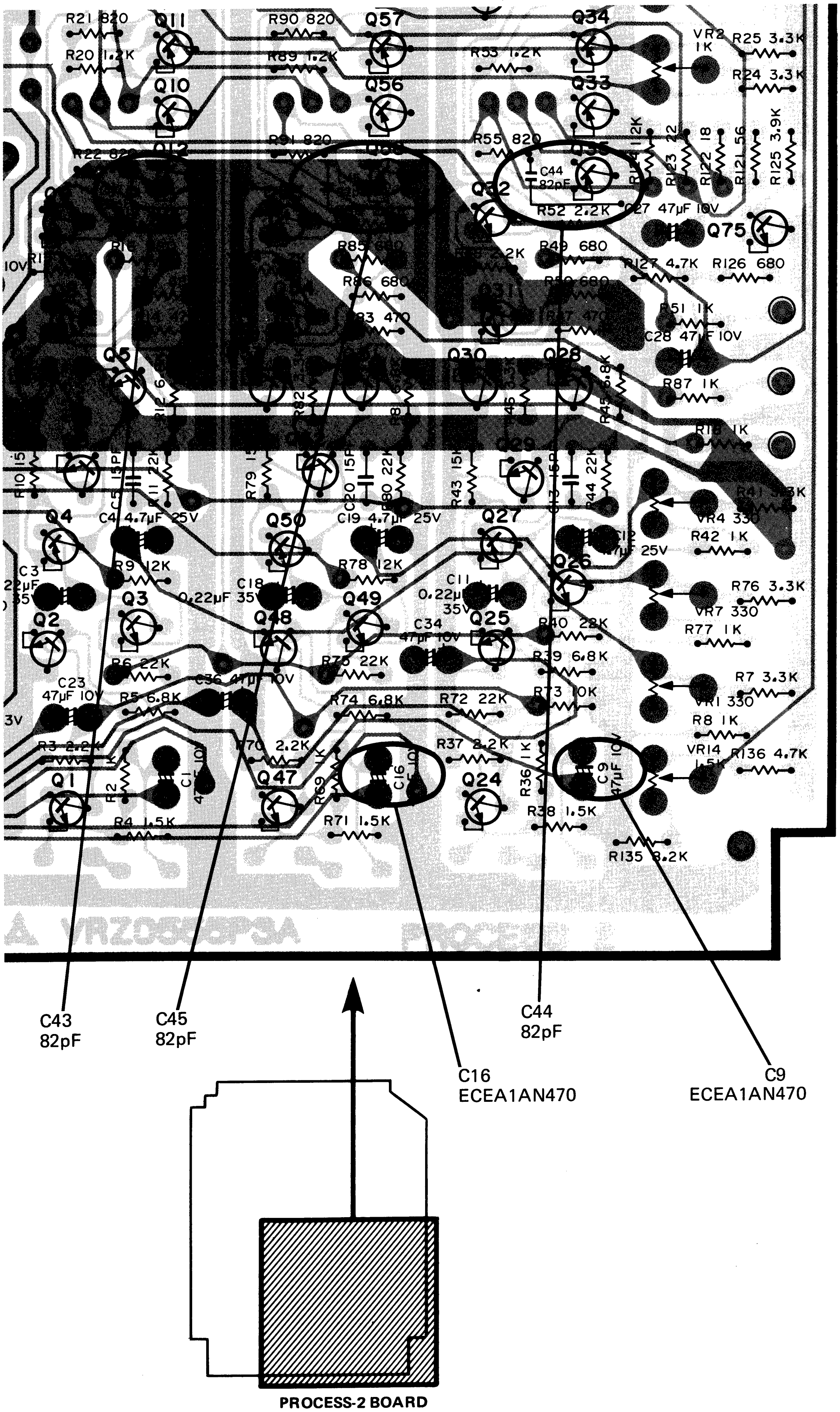

MOTHER BOARD


C22
2200pF
D11
D2
R42 100K
R5 47K
R7 47K
C6
0.047µF
C4 0.22µF
C2 0.22µF
C5
Q4
Q5
R16 75
R15 10K
C9 10µF 16V
R17 68
R14 1K
D1
Q12
R50 3.3K
C17 1000PF
Q15
C18 33µF 6.3V
R53
R54 15K
C16 33µF 6.3V
CN18
CN19
R58 68
R57 10K
R76 2.7K
R77 2.2K
R82 3.3K
R83 3.3K
R49 22K
R59 68
R60 10K
D15
D14
Q17
Q18
R80 2.2K
R78 100
D16
C15 33µF 6.3V
Q10
R44 5K
C23 33µF 25V
IC9
47µF 10V
R73 3.3K
R74 3.3K
R72 1K
R71 680
VR1 1K
R127 56K
C35 1µF 50V

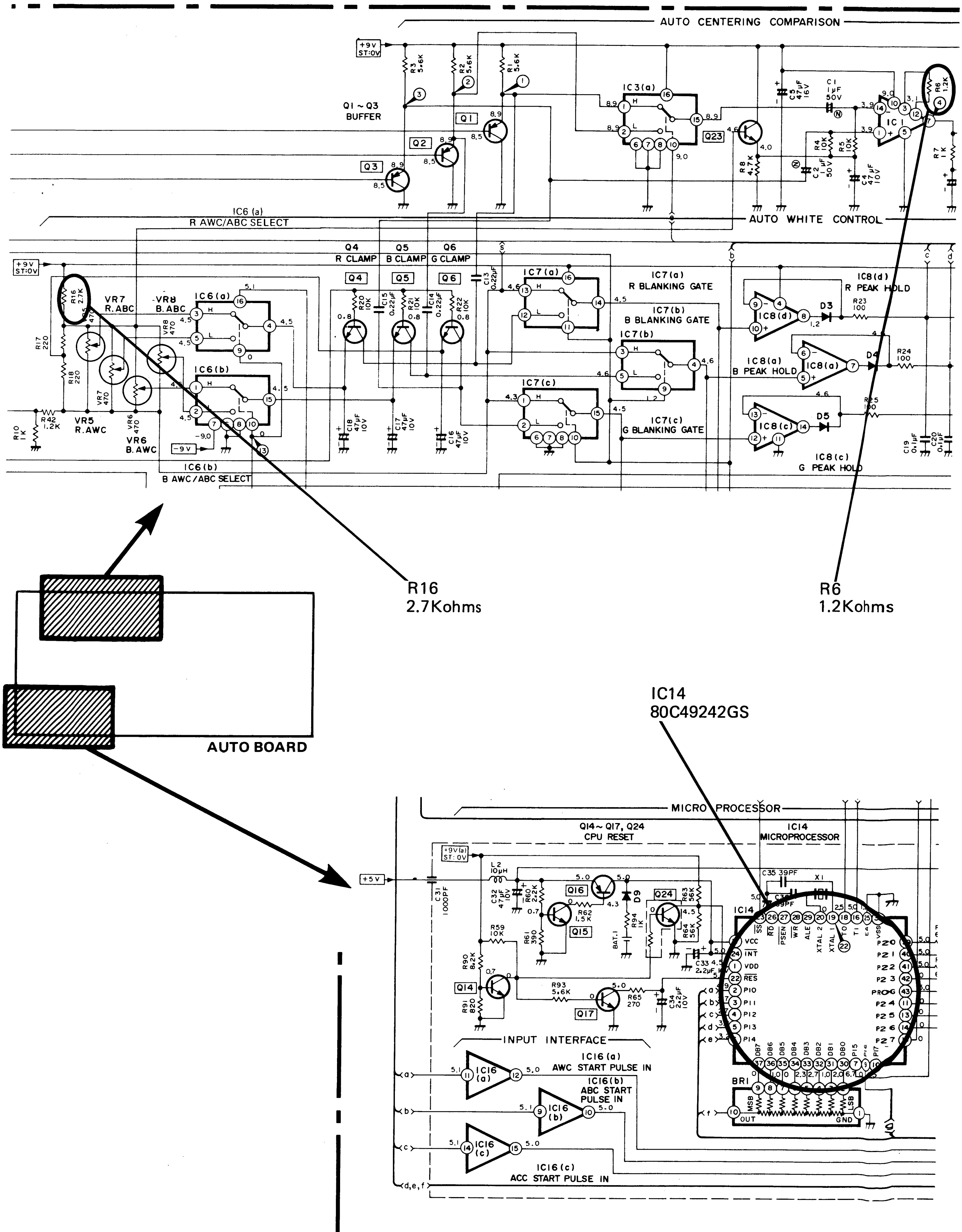

MOTHER BOARD

4-2 Process-2 Board


Q1, Q2 DETAIL MIX AMP
Q3 CLAMP
Q4 AMP
Q5 PRE BLANKING AMP
Q10~Q17 GAMMA CORRECTION BLACK
B SIGNAL PROCESSING
VR1 B PEDESTAL
Q6~Q9 AMP
Q24, Q25 DETAIL MIX AMP
Q26 CLAMP
Q27 AMP
G SIGNAL PROCESSING
Q33~Q40 GAMMA CORRECTION BLACK CLIP
Q29~Q32 AMP
VR4 G PEDESTAL
Q47, Q48 DETAIL MIX AMP
Q49 CLAMP
Q50 AMP
Q51 PRE BLANKING MIX
Q56~Q64 GAMMA CORRECTION BLACK CLIP
R SIGNAL PROCESSING
Q52~Q55 AMP
VR7 R PEDESTAL
+9V ST:OV
TP4
TP5
TP6
C43 82pF
C44 82pF
C45 82pF
C9 47μF10V
C16 47μF10V
C16 ECEA1AN470
C9 ECEA1AN470
C43 82pF
C44 82pF
C45 82pF
PROCESS-2 BOARD


C43
82pF
C45
82pF
C44
82pF
C16
ECEA1AN470
C9
ECEA1AN470
PROCESS-2 BOARD

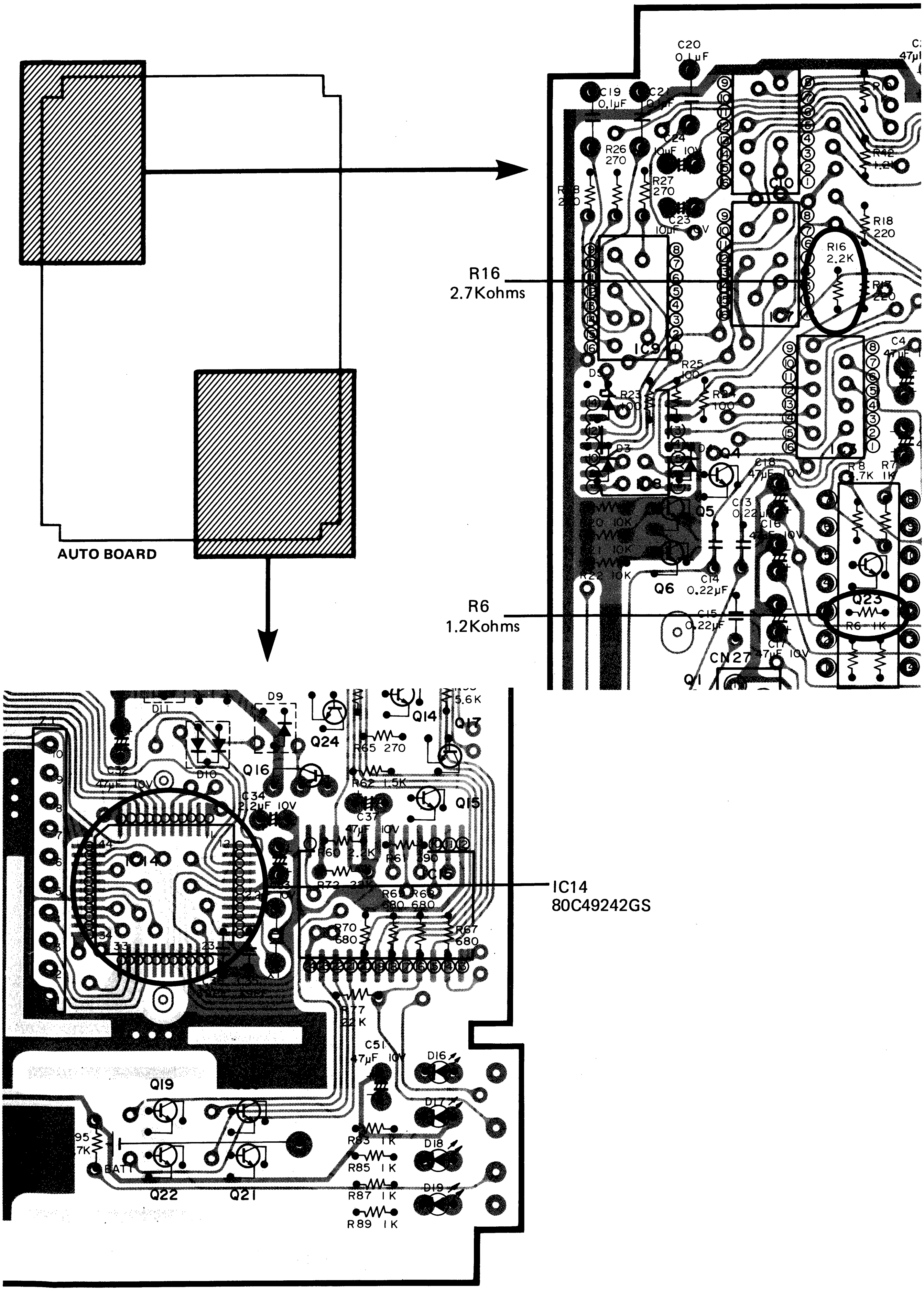
4-3 Auto Board


AUTO CENTERING COMPARISON
Q1 ~ Q3 BUFFER
Q1
Q2
Q3
Q23
IC3(a)
IC1
AUTO WHITE CONTROL
IC6 (a) R AWC/ABC SELECT
Q4 R CLAMP
Q5 B CLAMP
Q6 G CLAMP
IC6(a)
IC6(b)
IC7(a)
IC7(a) R BLANKING GATE
IC7(b) B BLANKING GATE
IC7(b)
IC7(c)
IC7(c) G BLANKING GATE
IC8(d) R PEAK HOLD
IC8(a) B PEAK HOLD
IC8(c) G PEAK HOLD
D3
D4
D5
VR7 R.ABC
VR8 B.ABC
VR5 R.AWC
VR6 B.AWC
IC6(b) B AWC/ABC SELECT
AUTO BOARD
MICRO PROCESSOR
Q14~Q17, Q24 CPU RESET
IC14 MICROPROCESSOR
Q14
Q15
Q16
Q17
Q24
INPUT INTERFACE
IC16(a) AWC START PULSE IN
IC16(b) ABC START PULSE IN
IC16(c) ACC START PULSE IN
BR1
+9V ST:0V
+5V

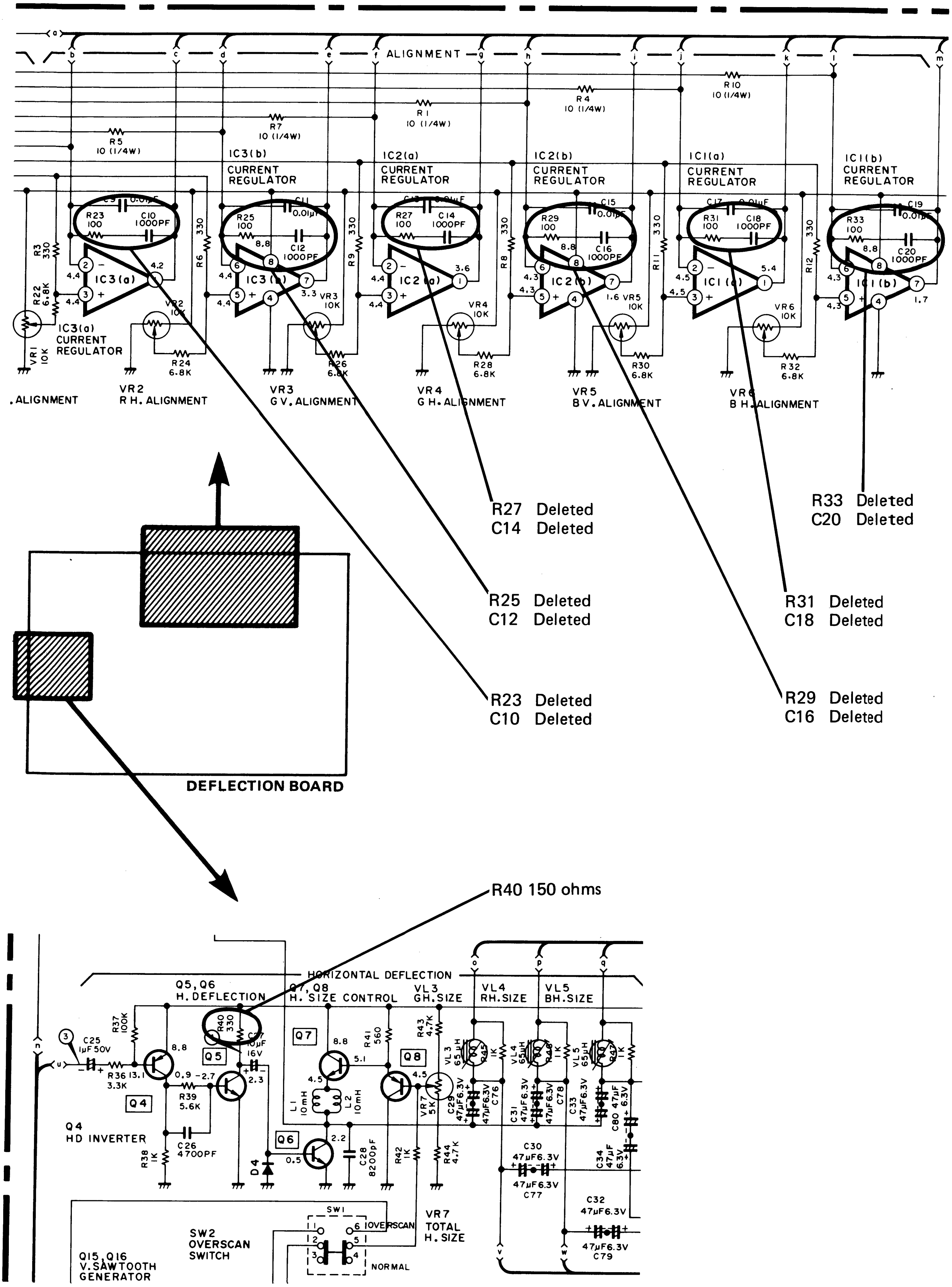
R16
2.7Kohms

R6
1.2Kohms

IC14
80C49242GS


AUTO BOARD
R16
2.7Kohms
R6
1.2Kohms
IC14
80C49242GS
R16
2.2K
R6 1K
Q23
IC7
IC9
IC10
IC14

4-4 Deflection Board


ALIGNMENT
R5 10 (1/4W)
R7 10 (1/4W)
R1 10 (1/4W)
R4 10 (1/4W)
R10 10 (1/4W)
IC3(b) CURRENT REGULATOR
IC2(a) CURRENT REGULATOR
IC2(b) CURRENT REGULATOR
IC1(a) CURRENT REGULATOR
IC1(b) CURRENT REGULATOR
R23 100
C10 1000PF
R25 100
C12 1000PF
R27 100
C14 1000PF
R29 100
C16 1000PF
R31 100
C18 1000PF
R33 100
C20 1000PF
R3 330
R22 6.8K
VR1 10K
IC3(a) CURRENT REGULATOR
R24 6.8K
R26 6.8K
R28 6.8K
R30 6.8K
R32 6.8K
VR2 10K
VR3 10K
VR4 10K
VR5 10K
VR6 10K
.ALIGNMENT
VR2 R H. ALIGNMENT
VR3 G V. ALIGNMENT
VR4 G H. ALIGNMENT
VR5 B V. ALIGNMENT
VR6 B H. ALIGNMENT
DEFLECTION BOARD
HORIZONTAL DEFLECTION
Q5, Q6 H. DEFLECTION
Q7, Q8 H. SIZE CONTROL
VL3 GH.SIZE
VL4 RH.SIZE
VL5 BH.SIZE
Q4 HD INVERTER
C25 1μF 50V
R36 3.3K
R37 100K
R38 1K
R39 5.6K
C26 4700PF
R40 330
C27 10μF 16V
R41 560
R42 1K
R43 4.7K
R44 4.7K
L1 10mH
L2 10mH
C28 8200pF
D4
VR7 5K
VL3 65μH
VL4 65μH
VL5 65μH
R45 1K
R46 1K
R47 1K
C29 47μF6.3V
C76 47μF6.3V
C31 47μF6.3V
C78 47μF6.3V
C33 47μF6.3V
C80 47μF 6.3V
C30 47μF6.3V
C77 47μF6.3V
C34 47μF 6.3V
C32 47μF6.3V
C79 47μF6.3V
SW1
OVERSCAN
NORMAL
SW2 OVERSCAN SWITCH
VR7 TOTAL H. SIZE
Q15, Q16 V.SAWTOOTH GENERATOR

R27 Deleted
C14 Deleted

R33 Deleted
C20 Deleted

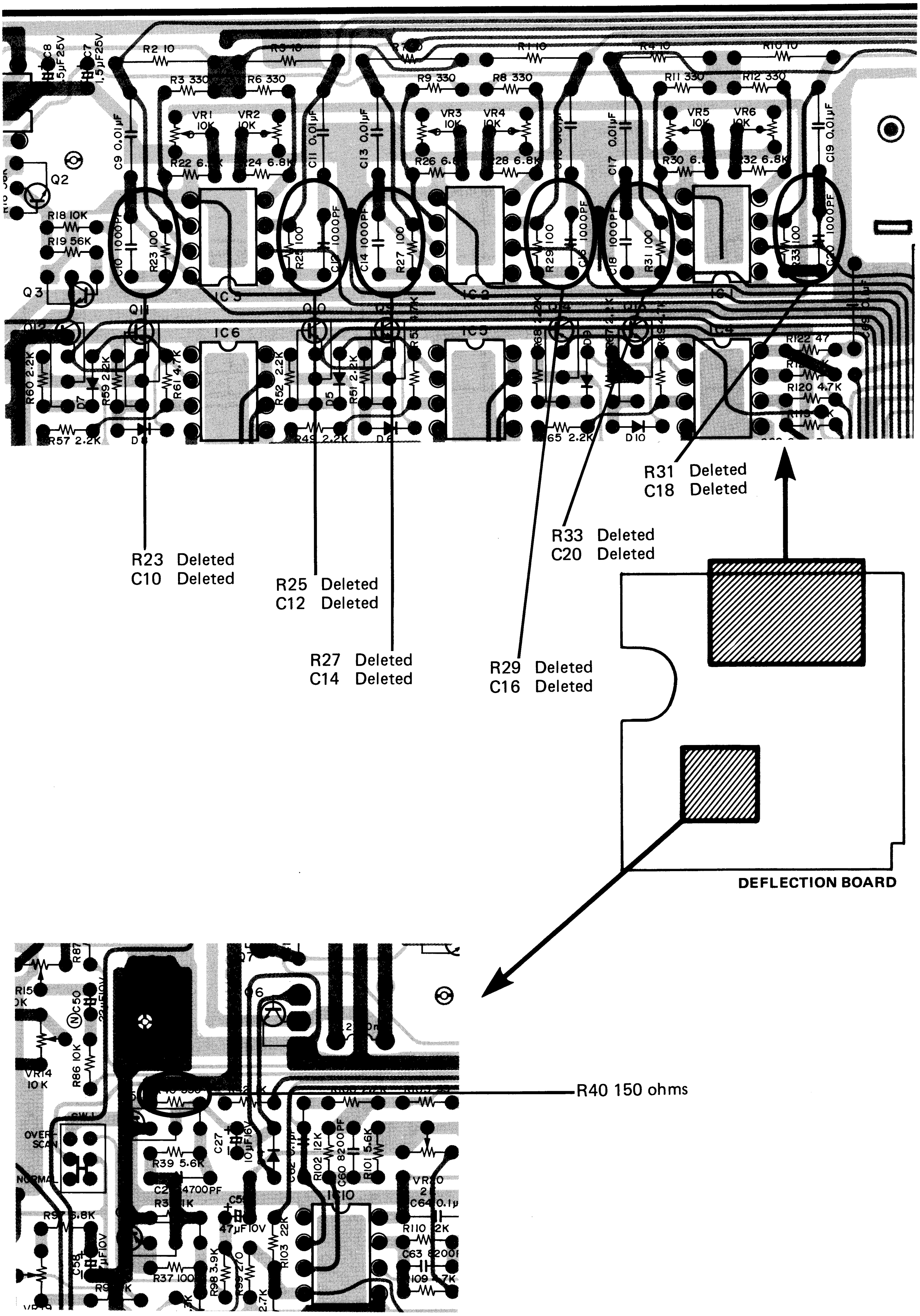
R25 Deleted
C12 Deleted

R31 Deleted
C18 Deleted

R23 Deleted
C10 Deleted

R29 Deleted
C16 Deleted

R40 150 ohms


DEFLECTION BOARD

R23 Deleted
C10 Deleted

R25 Deleted
C12 Deleted

R27 Deleted
C14 Deleted

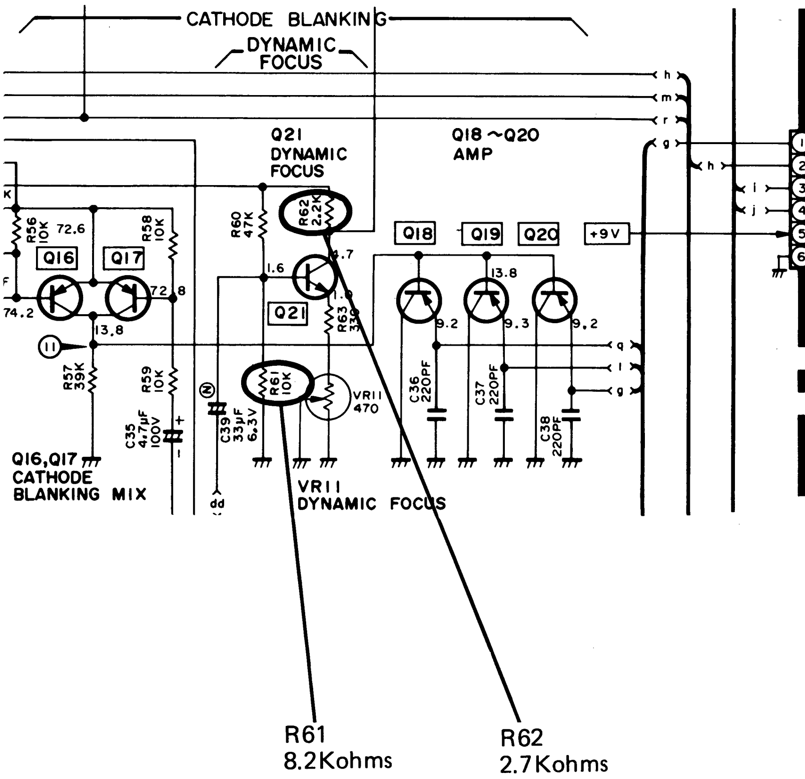
R29 Deleted
C16 Deleted

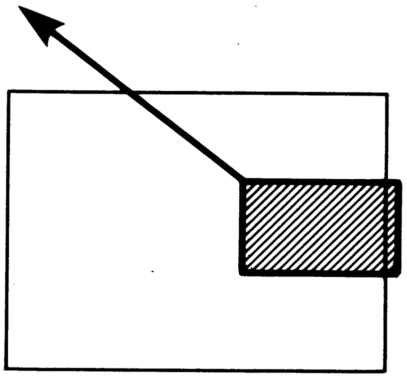
R33 Deleted
C20 Deleted

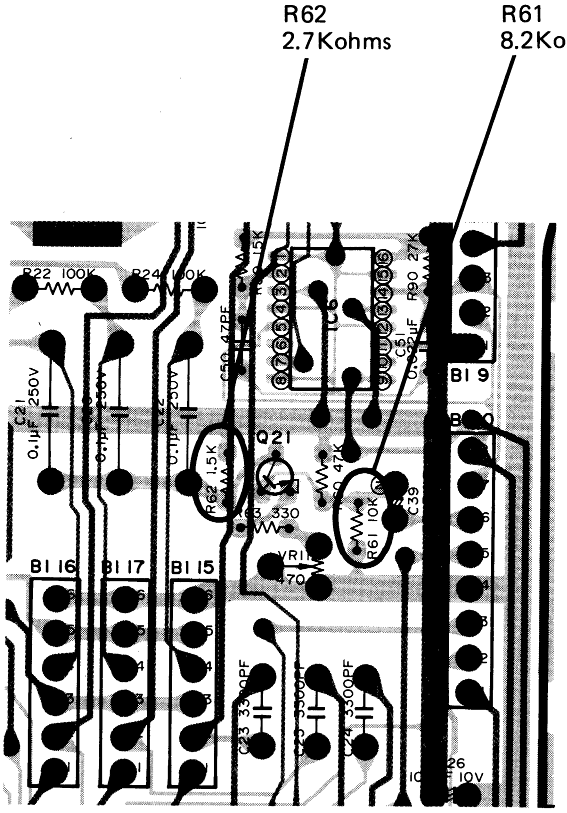
R31 Deleted
C18 Deleted

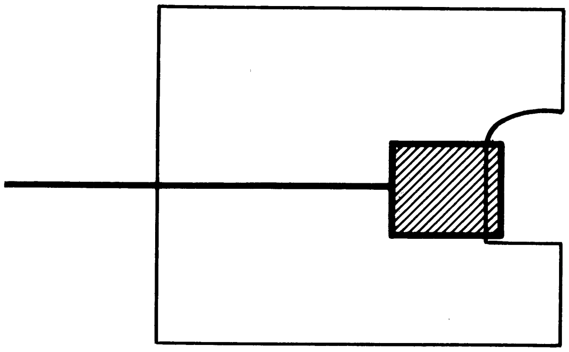
R40 150 ohms

4-5 High Voltage AIC Board

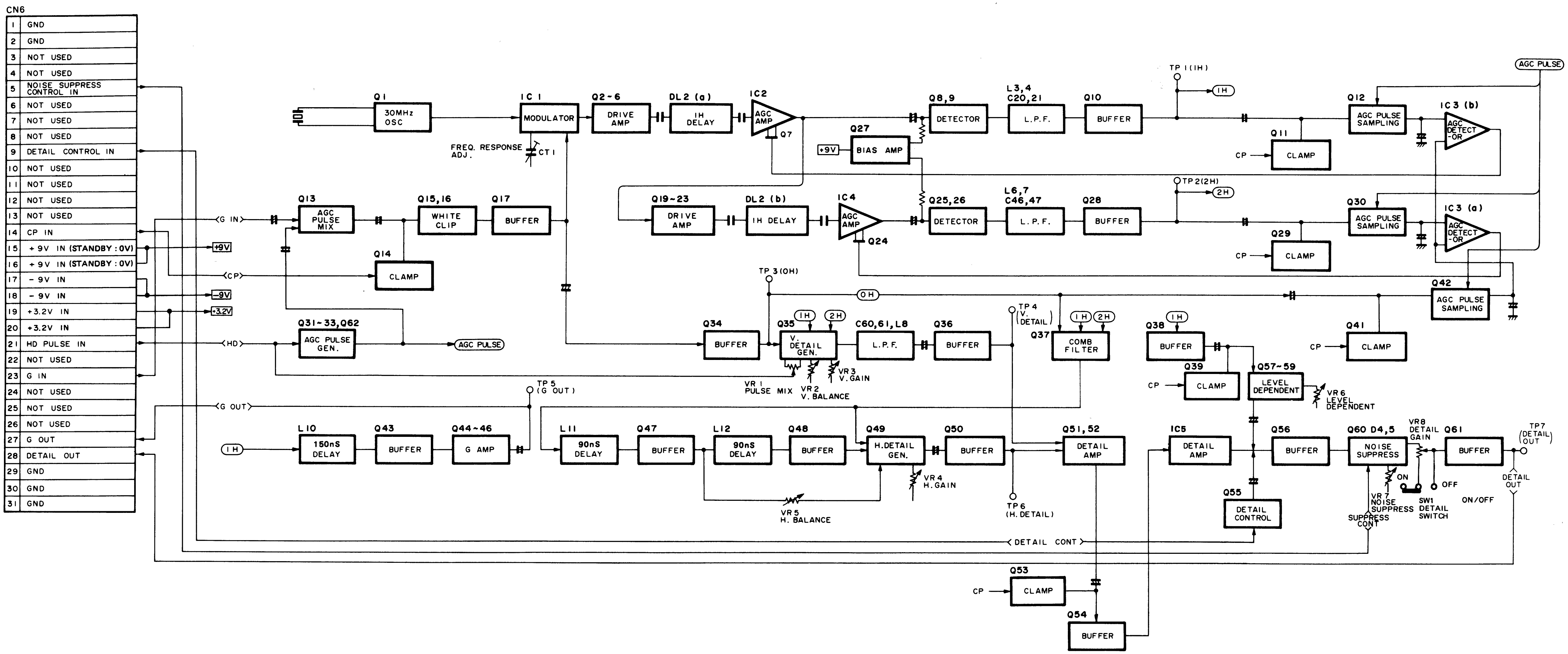

CATHODE BLANKING
DYNAMIC FOCUS
Q21 DYNAMIC FOCUS
Q18 ~Q20 AMP
R56 10K
72.6
R58 10K
Q16
Q17
74.2
72
8
13.8
11
R57 39K
R59 10K
C35 4.7μF 100V
Q16,Q17 CATHODE BLANKING MIX
R60 47K
R62 2.2K
1.6
4.7
Q21
R63 330
N
C39 33μF 6.3V
R61 10K
VR11 470
VR11 DYNAMIC FOCUS
dd
Q18
Q19
Q20
+9V
13.8
9.2
9.3
9.2
C36 220PF
C37 220PF
C38 220PF
h
m
r
g
q
i
j
B115
1 B K
2 B G1
3 B G2
4 B G3
5 B H(+)
6 B H(-)
R61 8.2Kohms
R62 2.7Kohms


HIGH VOLTAGE AIC BOARD


R62 2.7Kohms
R61 8.2Kohms
R22 100K
R24 100K
IC6
R90 27K
C50 47PF
C51 0.022μF
C21 0.1μF 250V
B19
B20
Q21
R62 1.5K
R63 330
R60 47K
R61 10K
N
C39
VR11 470
B116
B117
B115
C23 3300PF
C25 3300PF
C24 3300PF
C26 10V


HIGH VOLTAGE AIC BOARD

BLOCK DIAGRAM OF DETAIL BOARD

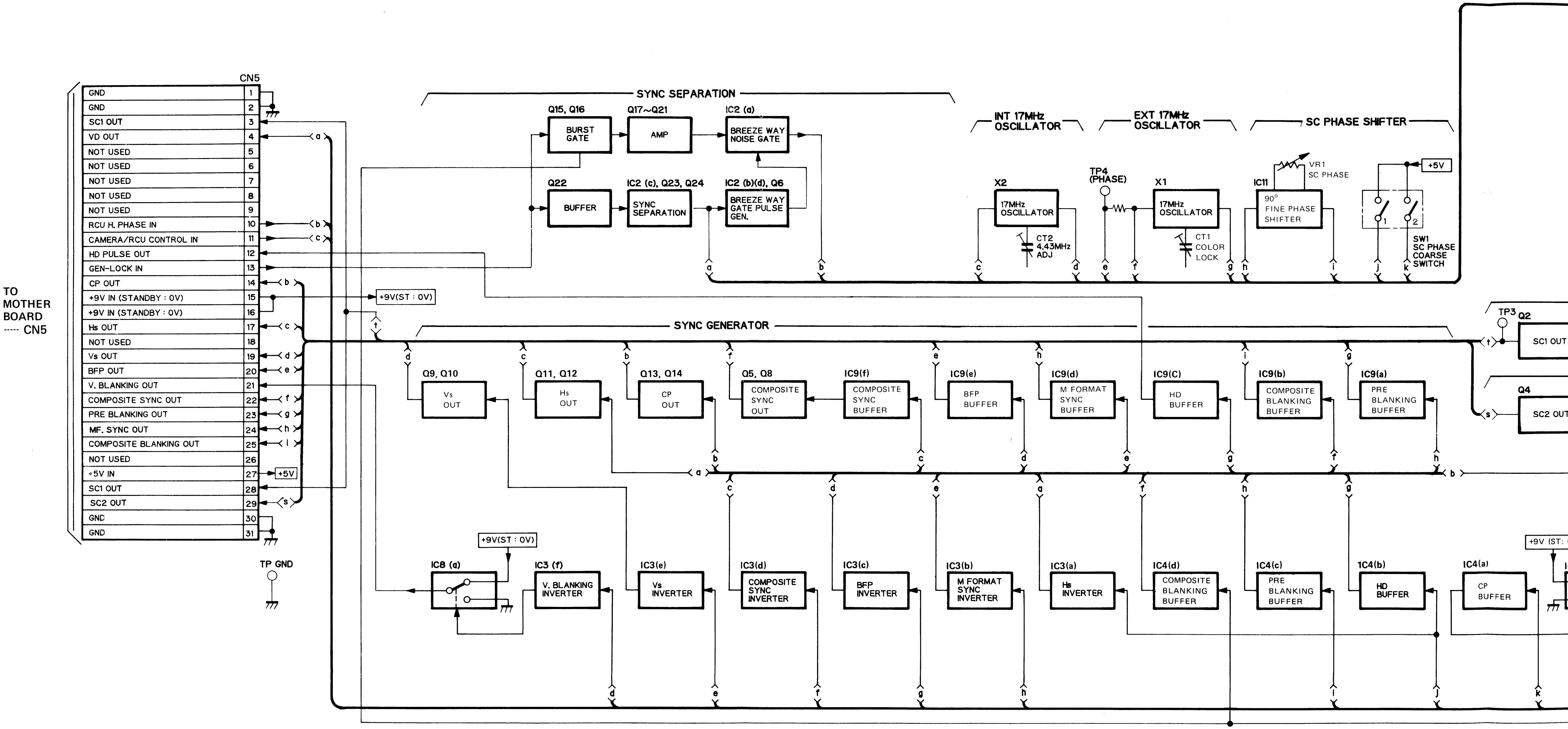


CN6

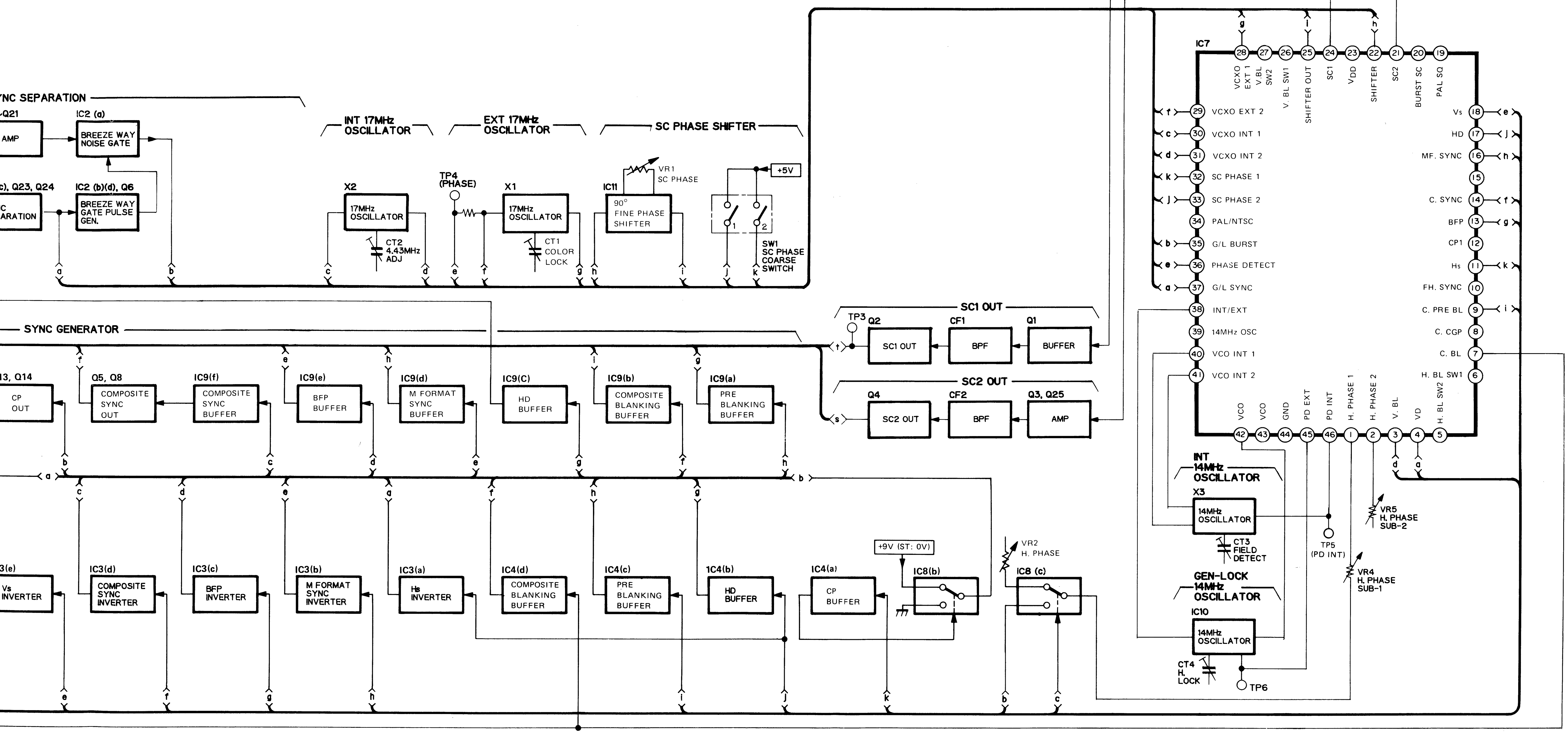
1	GND
2	GND
3	NOT USED
4	NOT USED
5	NOISE SUPPRESS CONTROL IN
6	NOT USED
7	NOT USED
8	NOT USED
9	DETAIL CONTROL IN
10	NOT USED
11	NOT USED
12	NOT USED
13	NOT USED
14	CP IN
15	+9V IN (STANDBY : 0V)
16	+9V IN (STANDBY : 0V)
17	-9V IN
18	-9V IN
19	+3.2V IN
20	+3.2V IN
21	HD PULSE IN
22	NOT USED
23	G IN
24	NOT USED
25	NOT USED
26	NOT USED
27	G OUT
28	DETAIL OUT
29	GND
30	GND
31	GND

Q1
30MHz OSC
IC 1
MODULATOR
FREQ. RESPONSE ADJ.
CT 1
Q2~6
DRIVE AMP
DL2 (a)
1H DELAY
IC2
AGC AMP
Q7
Q27
+9V
BIAS AMP
Q8,9
DETECTOR
L3,4 C20,21
L.P.F.
Q10
BUFFER
TP 1 (1H)
1H
AGC PULSE
Q11
CP
CLAMP
Q12
AGC PULSE SAMPLING
IC3 (b)
AGC DETECT -OR
G IN
Q13
AGC PULSE MIX
Q15,16
WHITE CLIP
Q17
BUFFER
Q14
CLAMP
+9V
CP
-9V
+3.2V
Q19~23
DRIVE AMP
DL2 (b)
1H DELAY
IC4
AGC AMP
Q24
Q25,26
DETECTOR
L6,7 C46,47
L.P.F.
Q28
BUFFER
TP2 (2H)
2H
Q29
CLAMP
Q30
AGC PULSE SAMPLING
IC3 (a)
AGC DETECT -OR
TP 3 (0H)
0H
Q42
AGC PULSE SAMPLING
Q41
CLAMP
HD
Q31~33, Q62
AGC PULSE GEN.
AGC PULSE
Q34
BUFFER
Q35
V. DETAIL GEN.
1H
2H
VR 1 PULSE MIX
VR 2 V. BALANCE
VR 3 V. GAIN
C60,61, L8
L.P.F.
Q36
BUFFER
TP 4 (V. DETAIL)
Q37
COMB FILTER
Q38
BUFFER
Q39
CLAMP
Q57~59
LEVEL DEPENDENT
VR 6 LEVEL DEPENDENT
TP 5 (G OUT)
G OUT
1H
L 10
150nS DELAY
Q43
BUFFER
Q44~46
G AMP
L11
90nS DELAY
Q47
BUFFER
L12
90nS DELAY
Q48
BUFFER
Q49
H. DETAIL GEN.
VR 4 H. GAIN
VR 5 H. BALANCE
Q50
BUFFER
TP 6 (H. DETAIL)
Q51,52
DETAIL AMP
IC5
DETAIL AMP
Q56
BUFFER
Q55
DETAIL CONTROL
Q60 D4,5
NOISE SUPPRESS
VR 7 NOISE SUPPRESS
SUPPRESS CONT
VR8 DETAIL GAIN
ON
OFF
SW1 DETAIL SWITCH
ON/OFF
Q61
BUFFER
TP7 (DETAIL OUT)
DETAIL OUT
DETAIL CONT
Q53
CLAMP
Q54
BUFFER

BLOCK DIAGRAM OF SYNC BOARD

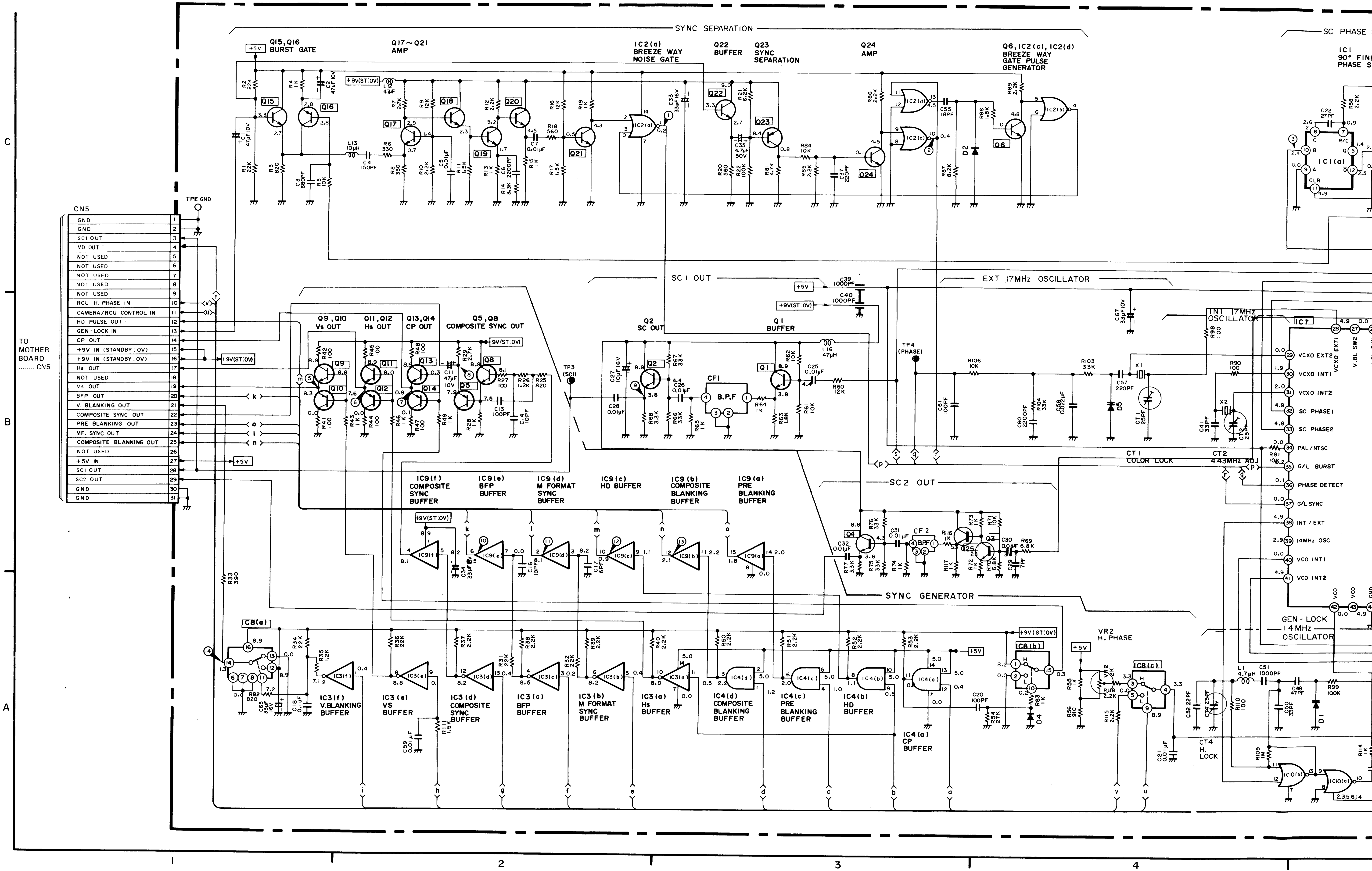

TO
MOTHER
BOARD
----- CN5
CN5
GND 1
GND 2
SC1 OUT 3
VD OUT 4
NOT USED 5
NOT USED 6
NOT USED 7
NOT USED 8
NOT USED 9
RCU H. PHASE IN 10
CAMERA/RCU CONTROL IN 11
HD PULSE OUT 12
GEN-LOCK IN 13
CP OUT 14
+9V IN (STANDBY : 0V) 15
+9V IN (STANDBY : 0V) 16
Hs OUT 17
NOT USED 18
Vs OUT 19
BFP OUT 20
V. BLANKING OUT 21
COMPOSITE SYNC OUT 22
PRE BLANKING OUT 23
MF. SYNC OUT 24
COMPOSITE BLANKING OUT 25
NOT USED 26
+5V IN 27
SC1 OUT 28
SC2 OUT 29
GND 30
GND 31
+5V
+9V(ST : 0V)
TP GND
SYNC SEPARATION
Q15, Q16
BURST GATE
Q17~Q21
AMP
IC2 (a)
BREEZE WAY NOISE GATE
Q22
BUFFER
IC2 (c), Q23, Q24
SYNC SEPARATION
IC2 (b)(d), Q6
BREEZE WAY GATE PULSE GEN.
INT 17MHz OSCILLATOR
X2
17MHz OSCILLATOR
CT2
4.43MHz ADJ
TP4
(PHASE)
EXT 17MHz OSCILLATOR
X1
17MHz OSCILLATOR
CT1
COLOR LOCK
SC PHASE SHIFTER
IC11
VR1
SC PHASE
90°
FINE PHASE SHIFTER
+5V
SW1
SC PHASE COARSE SWITCH
1
2
SYNC GENERATOR
Q9, Q10
Vs OUT
Q11, Q12
Hs OUT
Q13, Q14
CP OUT
Q5, Q8
COMPOSITE SYNC OUT
IC9(f)
COMPOSITE SYNC BUFFER
IC9(e)
BFP BUFFER
IC9(d)
M FORMAT SYNC BUFFER
IC9(C)
HD BUFFER
IC9(b)
COMPOSITE BLANKING BUFFER
IC9(a)
PRE BLANKING BUFFER
TP3
Q2
SC1 OUT
Q4
SC2 OUT
IC8 (a)
+9V(ST : 0V)
IC3 (f)
V. BLANKING INVERTER
IC3(e)
Vs INVERTER
IC3(d)
COMPOSITE SYNC INVERTER
IC3(c)
BFP INVERTER
IC3(b)
M FORMAT SYNC INVERTER
IC3(a)
Hs INVERTER
IC4(d)
COMPOSITE BLANKING BUFFER
IC4(c)
PRE BLANKING BUFFER
IC4(b)
HD BUFFER
IC4(a)
CP BUFFER
+9V (ST:
a
b
c
d
e
f
g
h
i
j
k
s
t

BLOCK DIAGRAM OF SYNC BOARD

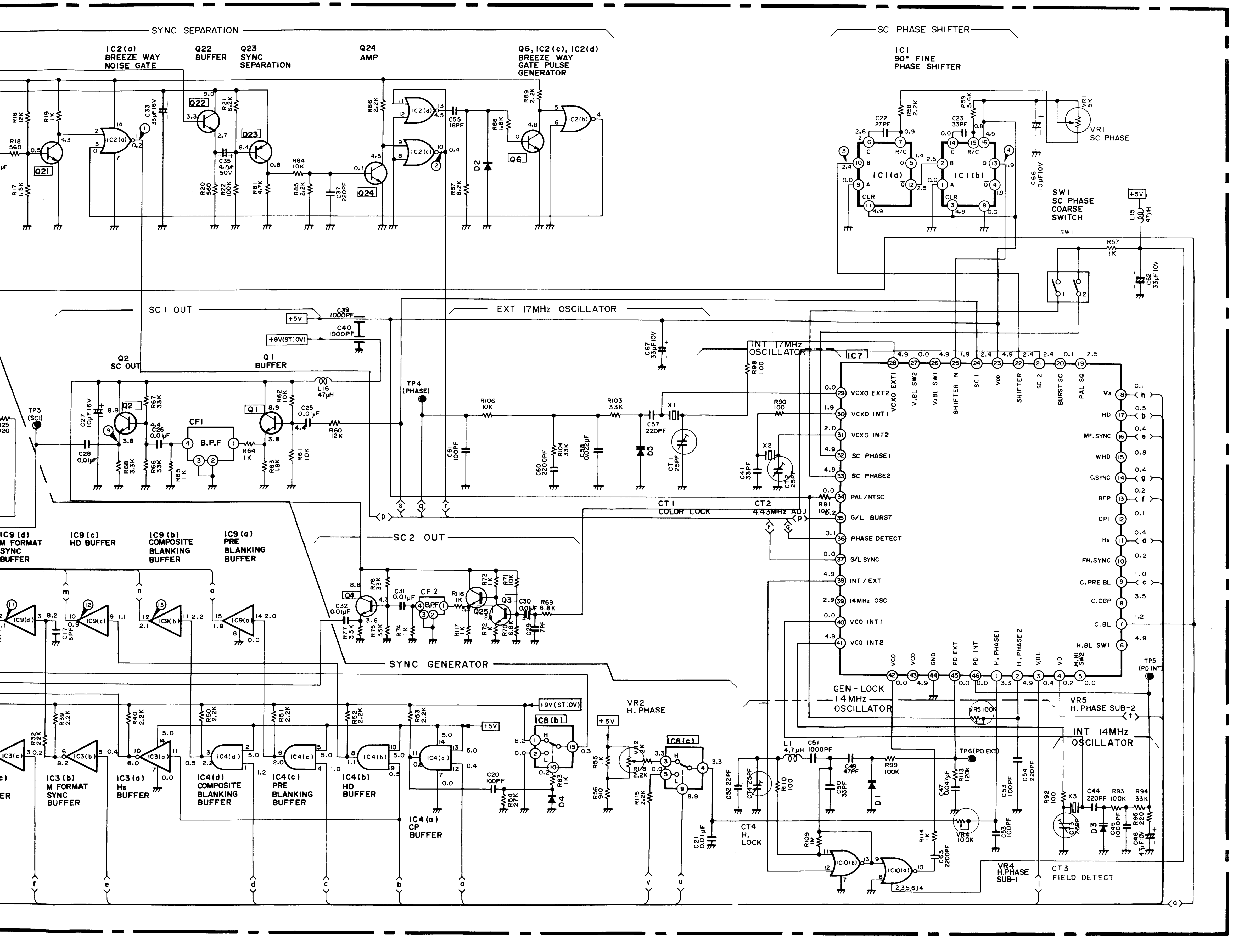


YNC SEPARATION
-Q21
AMP
IC2 (a)
BREEZE WAY NOISE GATE
c), Q23, Q24
C ARATION
IC2 (b)(d), Q6
BREEZE WAY GATE PULSE GEN.
INT 17MHz OSCILLATOR
X2
17MHz OSCILLATOR
CT2 4.43MHz ADJ
EXT 17MHz OSCILLATOR
TP4 (PHASE)
X1
17MHz OSCILLATOR
CT1 COLOR LOCK
SC PHASE SHIFTER
IC11
VR1 SC PHASE
90° FINE PHASE SHIFTER
+5V
SW1 SC PHASE COARSE SWITCH
SYNC GENERATOR
13, Q14
CP OUT
Q5, Q8
COMPOSITE SYNC OUT
IC9(f)
COMPOSITE SYNC BUFFER
IC9(e)
BFP BUFFER
IC9(d)
M FORMAT SYNC BUFFER
IC9(C)
HD BUFFER
IC9(b)
COMPOSITE BLANKING BUFFER
IC9(a)
PRE BLANKING BUFFER
3(e)
Vs INVERTER
IC3(d)
COMPOSITE SYNC INVERTER
IC3(c)
BFP INVERTER
IC3(b)
M FORMAT SYNC INVERTER
IC3(a)
Hs INVERTER
IC4(d)
COMPOSITE BLANKING BUFFER
IC4(c)
PRE BLANKING BUFFER
1C4(b)
HD BUFFER
IC4(a)
CP BUFFER
+9V (ST: 0V)
IC8(b)
VR2 H. PHASE
IC8 (c)
SC1 OUT
TP3
Q2
SC1 OUT
CF1
BPF
Q1
BUFFER
SC2 OUT
Q4
SC2 OUT
CF2
BPF
Q3, Q25
AMP
IC7
28 VCXO EXT 1
27 V BL SW2
26 V. BL SW1
25 SHIFTER OUT
24 SC1
23 VDD
22 SHIFTER
21 SC2
20 BURST SC
19 PAL SQ
29 VCXO EXT 2
30 VCXO INT 1
31 VCXO INT 2
32 SC PHASE 1
33 SC PHASE 2
34 PAL/NTSC
35 G/L BURST
36 PHASE DETECT
37 G/L SYNC
38 INT/EXT
39 14MHz OSC
40 VCO INT 1
41 VCO INT 2
18 Vs
17 HD
16 MF. SYNC
15
14 C. SYNC
13 BFP
12 CP1
11 Hs
10 FH. SYNC
9 C. PRE BL
8 C. CGP
7 C. BL
6 H. BL SW1
42 VCO
43 VCO
44 GND
45 PD EXT
46 PD INT
1 H. PHASE 1
2 H. PHASE 2
3 V. BL
4 VD
5 H. BL SW2
INT 14MHz OSCILLATOR
X3
14MHz OSCILLATOR
CT3 FIELD DETECT
TP5 (PD INT)
VR5 H. PHASE SUB-2
VR4 H. PHASE SUB-1
GEN-LOCK 14MHz OSCILLATOR
IC10
14MHz OSCILLATOR
CT4 H. LOCK
TP6
a
b
c
d
e
f
g
h
i
j
k
s
t

SCHEMATIC DIAGRAM OF SYNC BOARD


SYNC SEPARATION
Q15, Q16 BURST GATE
Q17~Q21 AMP
IC2(a) BREEZE WAY NOISE GATE
Q22 BUFFER
Q23 SYNC SEPARATION
Q24 AMP
Q6, IC2(c), IC2(d) BREEZE WAY GATE PULSE GENERATOR
SC PHASE
IC1 90° FINE PHASE S
TPE GND
CN5
TO MOTHER BOARD CN5
GND 1
GND 2
SC1 OUT 3
VD OUT 4
NOT USED 5
NOT USED 6
NOT USED 7
NOT USED 8
NOT USED 9
RCU H. PHASE IN 10
CAMERA/RCU CONTROL IN 11
HD PULSE OUT 12
GEN-LOCK IN 13
CP OUT 14
+9V IN (STANDBY: OV) 15
+9V IN (STANDBY: OV) 16
Hs OUT 17
NOT USED 18
Vs OUT 19
BFP OUT 20
V. BLANKING OUT 21
COMPOSITE SYNC OUT 22
PRE BLANKING OUT 23
MF. SYNC OUT 24
COMPOSITE BLANKING OUT 25
NOT USED 26
+5V IN 27
SC1 OUT 28
SC2 OUT 29
GND 30
GND 31
Q9, Q10 Vs OUT
Q11, Q12 Hs OUT
Q13, Q14 CP OUT
Q5, Q8 COMPOSITE SYNC OUT
TP3 (SC1)
SC 1 OUT
Q2 SC OUT
Q1 BUFFER
CF1 B.P.F
TP4 (PHASE)
EXT 17MHz OSCILLATOR
INT 17MHz OSCILLATOR
IC7
VCXO EXT2
VCXO INT1
VCXO INT2
SC PHASE1
SC PHASE2
PAL/NTSC
G/L BURST
PHASE DETECT
G/L SYNC
INT/EXT
14MHz OSC
VCO INT1
VCO INT2
CT1 COLOR LOCK
CT2 4.43MHz ADJ
SC2 OUT
CF2 BPF
SYNC GENERATOR
IC9(f) COMPOSITE SYNC BUFFER
IC9(e) BFP BUFFER
IC9(d) M FORMAT SYNC BUFFER
IC9(c) HD BUFFER
IC9(b) COMPOSITE BLANKING BUFFER
IC9(a) PRE BLANKING BUFFER
IC8(a)
IC3(f) V.BLANKING BUFFER
IC3(e) VS BUFFER
IC3(d) COMPOSITE SYNC BUFFER
IC3(c) BFP BUFFER
IC3(b) M FORMAT SYNC BUFFER
IC3(a) Hs BUFFER
IC4(d) COMPOSITE BLANKING BUFFER
IC4(c) PRE BLANKING BUFFER
IC4(b) HD BUFFER
IC4(a) CP BUFFER
IC8(b)
VR2 H. PHASE
IC8(c)
CT4 H. LOCK
GEN-LOCK 14MHz OSCILLATOR
IC10(b)
IC10(a)
+5V
+9V(ST:OV)
C
B
A
1
2
3
4

SCHEMATIC DIAGRAM OF SYNC BOARD

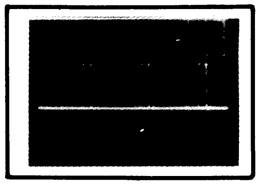


SYNC SEPARATION
IC2(a) BREEZE WAY NOISE GATE
Q22 BUFFER
Q23 SYNC SEPARATION
Q24 AMP
Q6, IC2(c), IC2(d) BREEZE WAY GATE PULSE GENERATOR
SC PHASE SHIFTER
IC1 90° FINE PHASE SHIFTER
VR1 SC PHASE
SW1 SC PHASE COARSE SWITCH
+5V
SC1 OUT
+9V(ST:0V)
Q2 SC OUT
Q1 BUFFER
TP3 (SC1)
TP4 (PHASE)
CF1 B.P.F
EXT 17MHz OSCILLATOR
INT 17MHz OSCILLATOR
IC7
VCXO EXT2
VCXO INT1
VCXO INT2
SC PHASE1
SC PHASE2
PAL/NTSC
G/L BURST
PHASE DETECT
G/L SYNC
INT/EXT
14MHz OSC
VCO INT1
VCO INT2
VCXO EXT1
V.BL SW2
V.BL SW1
SHIFTER IN
SC 1
Vcc
SHIFTER
SC 2
BURST SC
PAL SQ
Vs
HD
MF.SYNC
WHD
C.SYNC
BFP
CPI
Hs
FH.SYNC
C.PRE BL
C.CGP
C.BL
H.BL SW1
VCO
GND
PD EXT
PD INT
H.PHASE1
H.PHASE 2
VBL
VD
H.BL SW2
CT1 COLOR LOCK
CT2 4.43MHz ADJ
SC2 OUT
CF2 B.P.F
IC9(d) M FORMAT SYNC BUFFER
IC9(c) HD BUFFER
IC9(b) COMPOSITE BLANKING BUFFER
IC9(a) PRE BLANKING BUFFER
SYNC GENERATOR
IC3(b) M FORMAT SYNC BUFFER
IC3(a) Hs BUFFER
IC4(d) COMPOSITE BLANKING BUFFER
IC4(c) PRE BLANKING BUFFER
IC4(b) HD BUFFER
IC4(a) CP BUFFER
IC8(b)
IC8(c)
VR2 H. PHASE
GEN-LOCK 14MHz OSCILLATOR
VR5 H. PHASE SUB-2
INT 14MHz OSCILLATOR
TP5 (PD INT)
TP6 (PD EXT)
CT4 H. LOCK
VR4 H.PHASE SUB-1
CT3 FIELD DETECT
3
4
5

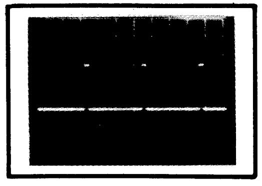
IC1	SN74LS221S		C5
IC2	TC40H002F		C2, C3, C4
IC3	DN74LS05S		A2, A3
IC4	DN74LS09S		A3
IC7	MP7260A		A5, B5
IC8	TC4053BF		A1, A4
IC9	TC4050BF		B2, B3
IC10	TC40H002F		A4, A5
Q1	2SD601-QRS	(Y)	B3
Q2	2SD601-QRS	(Y)	B2
Q3	2SD601-QRS	(Y)	B3
Q4	2SD601-QRS	(Y)	B3
Q5	2SB709-QRS	(A)	B2
Q6	2SD601-QRS	(Y)	C4
Q8	2SD601-QRS	(Y)	B2
Q9	2SD601-QRS	(Y)	B1
Q10	2SB709-QRS	(A)	B1
Q11	2SD601-QRS	(Y)	B2
Q12	2SB709-QRS	(A)	B2
Q13	2SD601-QRS	(Y)	B2
Q14	2SB709-QRS	(A)	B2
Q15	2SD601-QRS	(Y)	C1
Q16	2SB709-QRS	(A)	C1
Q17	2SD601-QRS	(Y)	C2
Q18	2SD601-QRS	(Y)	C2
Q19	2SD601-QRS	(Y)	C2
Q20	2SD601-QRS	(Y)	C2
Q21	2SC641K-C		C2
Q22	2SD601-QRS	(Y)	C3
Q23	2SB709-QRS	(A)	C3
Q24	2SC641K-C		C3
Q25	2SD601-QRS	(Y)	B3
D1	YUD1S2688		A5
D2	MA165		B4
D3	YUD1S2688		A5
D4	MA165		A4
D5	YUD1S2688		C4

SIGNAL WAVEFORMS OF SYNC BOARD

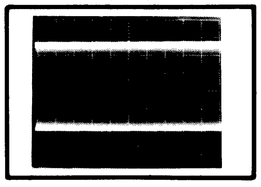
1 2.0V/DIV 20μs/DIV



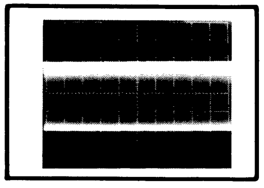
2 2.0V/DIV 20μs/DIV



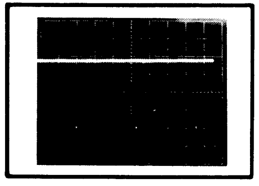
3 1V/DIV, 20μs/DIV



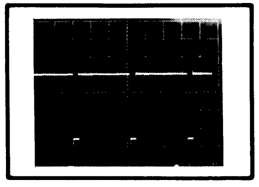
4 1V/DIV, 20μs/DIV



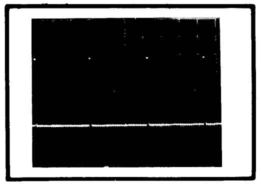
5 2V/DIV, 5ms/DIV



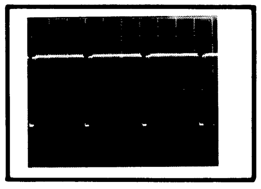
6 2V/DIV, 20μs/DIV



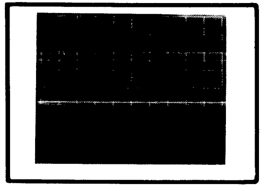
7 2V/DIV, 20μs/DIV



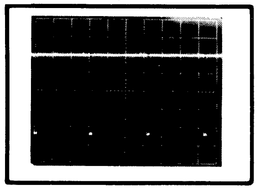
8 2V/DIV, 20μs/DIV



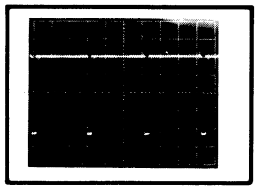
9 0.2V/DIV, 20μs/DIV



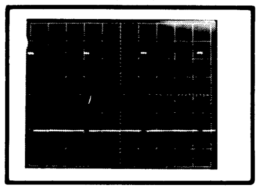
10 2V/DIV, 20μs/DIV



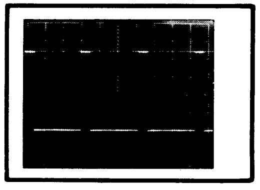
11 2V/DIV, 20μs/DIV



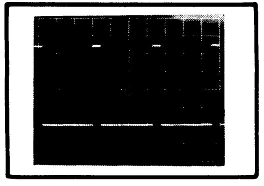
12 2V/DIV, 20μs/DIV



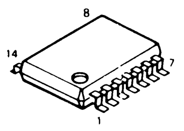
13 2V/DIV, 20μs/DIV



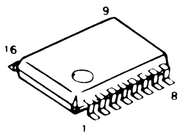
14 2V/DIV, 5ms/DIV



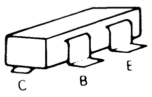
DN74LS05S
DN74LS09S
TC40H002F



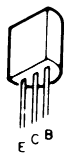
SN74LS221S
TC4050BF
TC4053BF



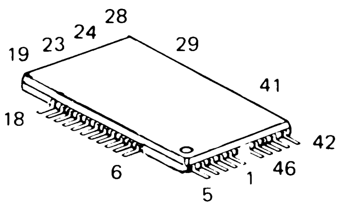
2SB709-QRS
2SD601-QRS



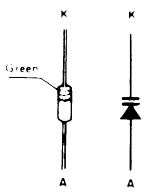
2SC641K-C



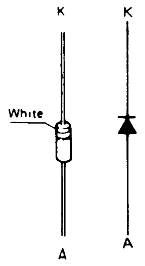
MP7260A


28
24
23
19
29
41
18
42
46
1
6
5

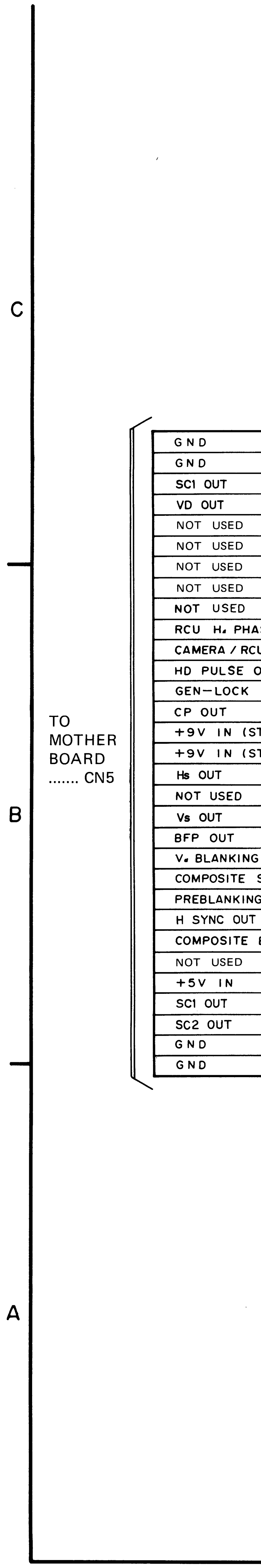
YUD1S2688



MA165

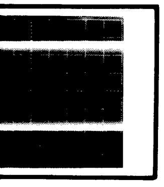


IC1	SN74LS221S		C3
IC2	TC40H002F		A3
IC3	DN74LS05S		C2
IC4	DN74LS09S		B2
IC7	MP7260A		B3, C3
IC8	TC4053BF		C2
IC9	TC4050BF		A2
IC10	TC40H002F		B3
Q1	2SD601-QRS	(Y)	C2
Q2	2SD601-QRS	(Y)	C2
Q3	2SD601-QRS	(Y)	B3
Q4	2SD601-QRS	(Y)	B3
Q5	2SB709-QRS	(A)	A2
Q6	2SD601-QRS	(Y)	A3
Q8	2SD601-QRS	(Y)	A2
Q9	2SD601-QRS	(Y)	A2
Q10	2SB709-QRS	(A)	A2
Q11	2SD601-QRS	(Y)	A2
Q12	2SB709-QRS	(A)	A2
Q13	2SD601-QRS	(Y)	A2
Q14	2SB709-QRS	(A)	A2
Q15	2SD601-QRS	(Y)	A2
Q16	2SB709-QRS	(A)	A3
Q17	2SD601-QRS	(Y)	A3
Q18	2SD601-QRS	(Y)	A3
Q19	2SD601-QRS	(Y)	A3
Q20	2SD601-QRS	(Y)	A3
Q21	2SC641K-C		A3
Q22	2SD601-QRS	(Y)	A2
Q23	2SB709-QRS	(A)	A2
Q24	2SC641K-C		A2
Q25	2SD601-QRS	(Y)	B3
D1	YUD1S2688		B2
D2	MA165		A3
D3	YUD1S2688		C3
D4	MA165		C2
D5	YUD1S2688		C3

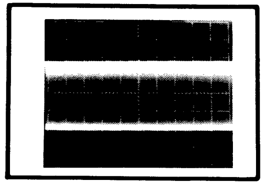

C
B
A
TO
MOTHER
BOARD
.... CN5
GND
GND
SC1 OUT
VD OUT
NOT USED
NOT USED
NOT USED
NOT USED
NOT USED
RCU H. PHA
CAMERA / RCU
HD PULSE O
GEN-LOCK
CP OUT
+9V IN (ST
+9V IN (ST
Hs OUT
NOT USED
Vs OUT
BFP OUT
V. BLANKING
COMPOSITE S
PREBLANKING
H SYNC OUT
COMPOSITE E
NOT USED
+5V IN
SC1 OUT
SC2 OUT
GND
GND

MS OF SYNC BOARD

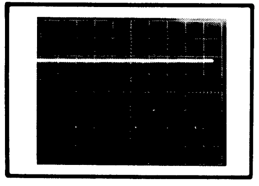
V, 20μs/DIV



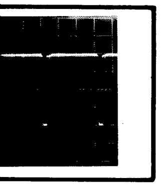
4 1V/DIV, 20μs/DIV



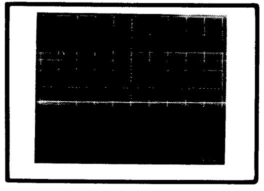
5 2V/DIV, 5ms/DIV



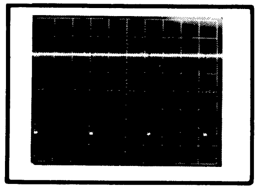
IV, 20μs/DIV



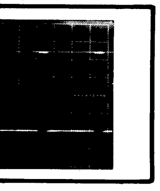
9 0.2V/DIV, 20μs/DIV



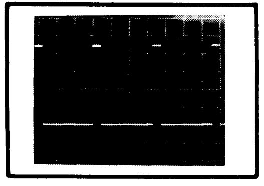
10 2V/DIV, 20μs/DIV



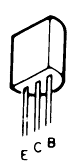
IV, 20μs/DIV



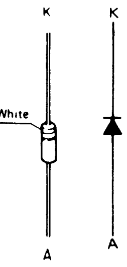
14 2V/DIV, 5ms/DIV



2SC641K-C



MA165



CONDUCTOR

SYNC BOARD

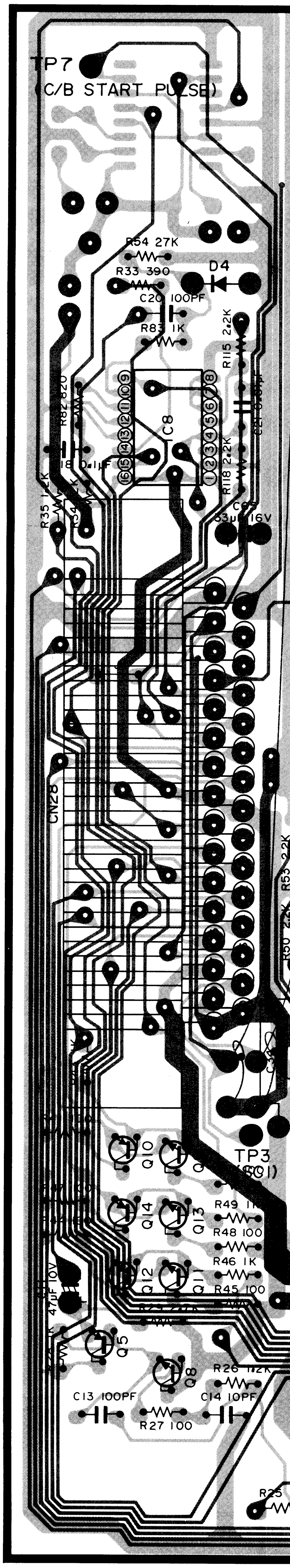
C

B

A

TO MOTHER BOARD CN5

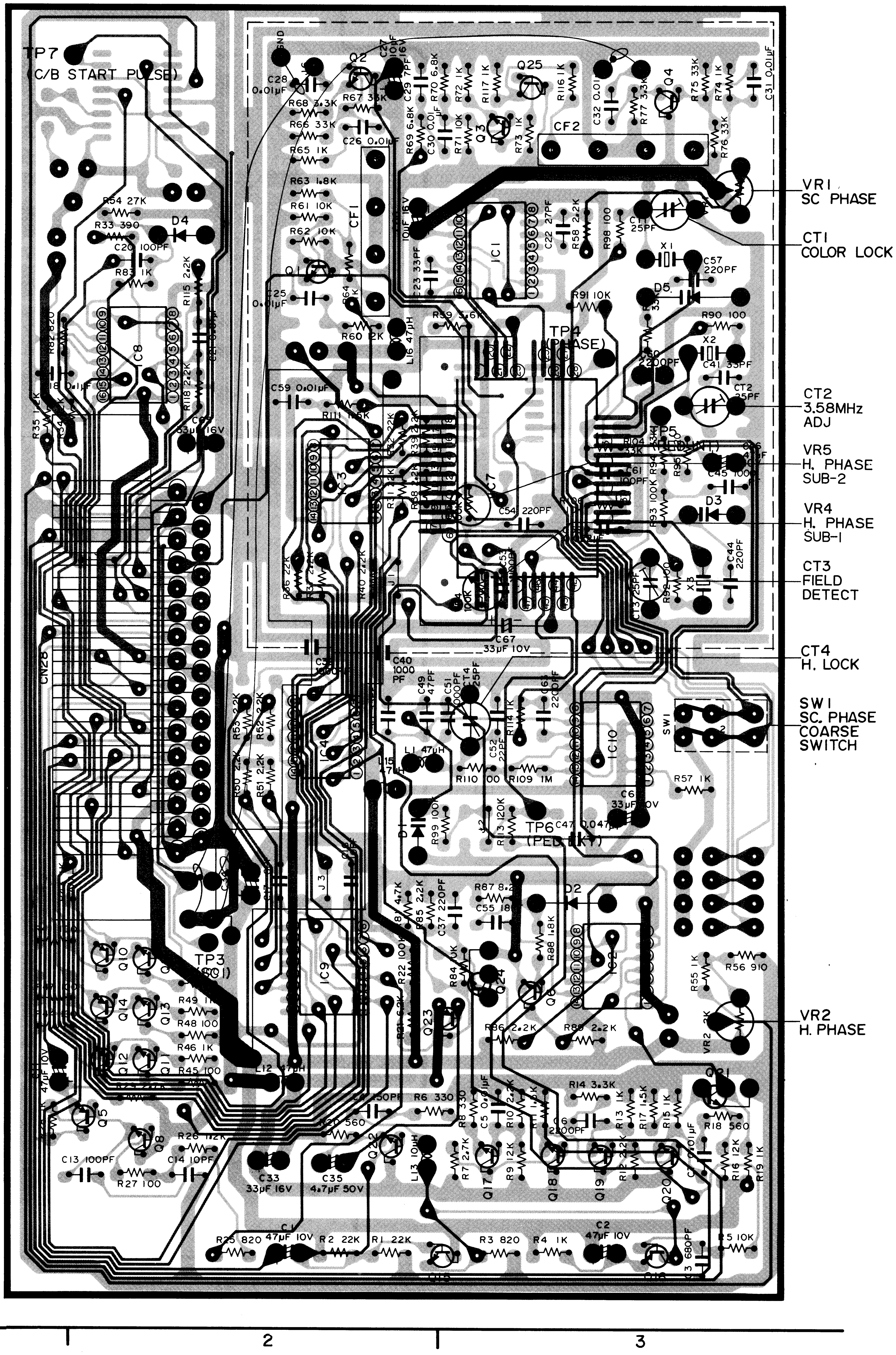
	CN5
GND	1
GND	2
SC1 OUT	3
VD OUT	4
NOT USED	5
NOT USED	6
NOT USED	7
NOT USED	8
NOT USED	9
RCU H. PHASE IN	10
CAMERA / RCU CONTROL IN	11
HD PULSE OUT	12
GEN-LOCK IN	13
CP OUT	14
+9V IN (STANDBY : 0V)	15
+9V IN (STANDBY : 0V)	16
Hs OUT	17
NOT USED	18
Vs OUT	19
BFP OUT	20
V. BLANKING OUT	21
COMPOSITE SYNC OUT	22
PREBLANKING OUT	23
H SYNC OUT	24
COMPOSITE BLANKING OUT	25
NOT USED	26
+5V IN	27
SC1 OUT	28
SC2 OUT	29
GND	30
GND	31


TP7
(C/B START PULSE)
R54 27K
R33 390
D4
C20 100PF
R83 1K
R115 2.2K
R82 820
IC8
R118 2.2K
R35 1.2K
C65 33μ 16V
CN28
R53 2.2K
R50 2.2K
TP3
(SC1)
Q10
Q9
Q14
Q13
Q12
Q11
R49 1K
R48 100
R46 1K
R45 100
47μF 10V
Q5
Q8
R26 1.2K
C13 100PF
C14 10PF
R27 100
R25

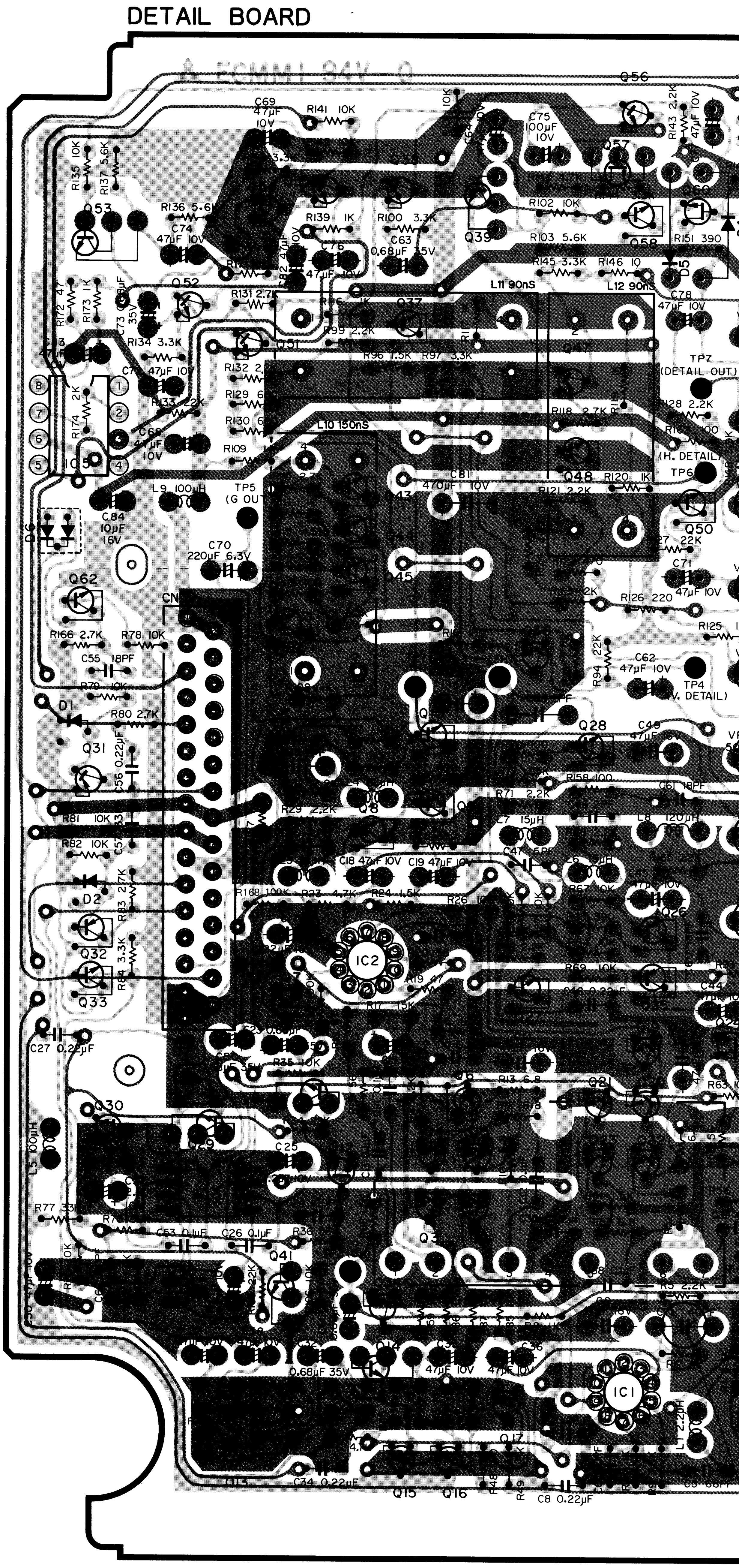
CONDUCTOR VIEW OF SYNC BOARD

SYNC BOARD

	CN5
	1
	2
UT	3
T	4
USED	5
USED	6
USED	7
USED	8
USED	9
H. PHASE IN	10
RA / RCU CONTROL IN	11
ULSE OUT	12
LOCK IN	13
OT	14
IN (STANDBY : OV)	15
IN (STANDBY : OV)	16
T	17
USED	18
T	19
UT	20
ANKING OUT	21
SITE SYNC OUT	22
ANKING OUT	23
C OUT	24
SITE BLANKING OUT	25
USED	26
IN	27
UT	28
UT	29
	30
	31


TP7 (C/B START PULSE)
TP4 (PHASE)
TP5
TP3
TP6 (PEDESTAL)
CN20
IC1
IC2
IC8
IC9
IC10
CF1
CF2
VR1 SC PHASE
CT1 COLOR LOCK
CT2 3.58MHz ADJ
VR5 H. PHASE SUB-2
VR4 H. PHASE SUB-1
CT3 FIELD DETECT
CT4 H. LOCK
SW1 SC. PHASE COARSE SWITCH
VR2 H. PHASE
1
2
3

CONDUCTOR VIEW OF DETAIL BOARD



DETAIL BOARD
Q56
Q53
Q52
Q51
Q37
Q39
Q58
Q60
Q47
Q48
Q50
Q62
Q31
Q32
Q33
Q28
Q26
Q30
Q41
Q13
Q15
Q16
Q17
IC1
IC2
IC5
D1
D2
D5
D6
L5 100μH
L9 100μH
L10 150nS
L11 90nS
L12 90nS
TP4 (V. DETAIL)
TP5 (G OUT)
TP6 (H. DETAIL)
TP7 (DETAIL OUT)
C70 220μF 6.3V
C75 100μF 10V
C84 10μF 16V
R135 10K
R137 5.6K
R141 10K
R102 10K
R103 5.6K
R145 3.3K
R146 10
R151 390
R166 2.7K
R78 10K
C55 18PF
R80 2.7K
R81 10K
R82 10K
R83 27K
R84 3.3K
C27 0.22μF
C34 0.22μF
C8 0.22μF

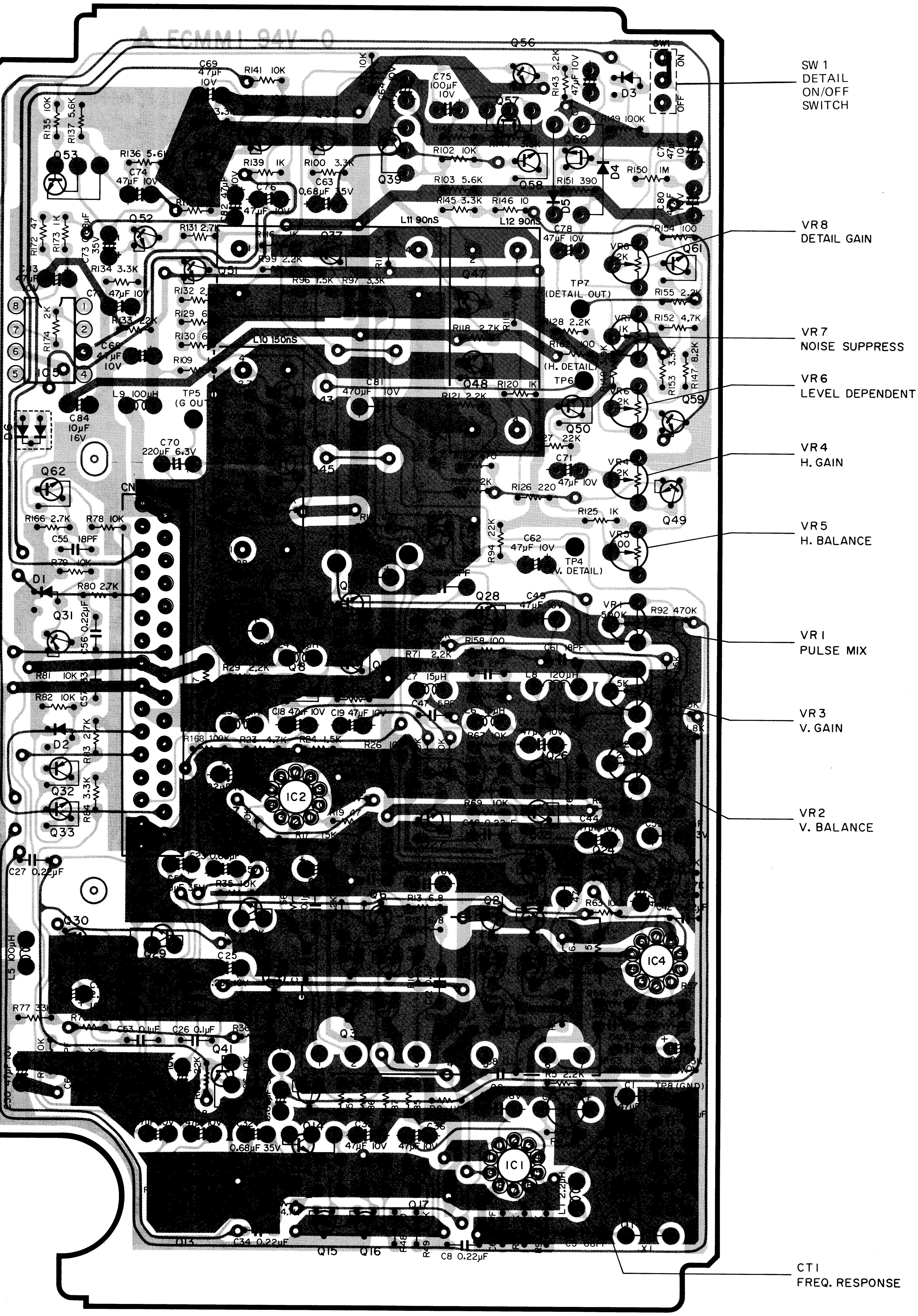
CN6

TO MOTHER BOARD ... CN6	GND	1
	GND	2
	NOT USED	3
	NOT USED	4
	NOISE SUPPRESS CONTROL IN	5
	NOT USED	6
	NOT USED	7
	NOT USED	8
	DETAIL CONTROL IN	9
	NOT USED	10
	NOT USED	11
	NOT USED	12
	NOT USED	13
	CP IN	14
	+9V IN (STANDBY : 0V)	15
	+9V IN (STANDBY : 0V)	16
	−9V IN	17
	−9V IN	18
	+3.2V IN	19
	NOT USED	20
	HD PULSE IN	21
	NOT USED	22
	G IN	23
	NOT USED	24
	GND	25
	NOT USED	26
	G OUT	27
	DETAIL OUT	28
	GND	29
	GND	30
	GND	31

C
B
A
1
2

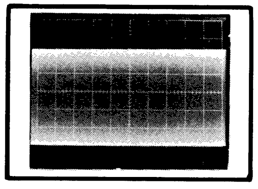
CONDUCTOR VIEW OF DETAIL BOARD

DETAIL BOARD

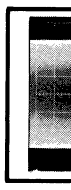

SW 1
DETAIL
ON/OFF
SWITCH
VR8
DETAIL GAIN
VR7
NOISE SUPPRESS
VR6
LEVEL DEPENDENT
VR4
H. GAIN
VR5
H. BALANCE
VR I
PULSE MIX
VR3
V. GAIN
VR2
V. BALANCE
CT I
FREQ. RESPONSE
2
3

SIGNAL V

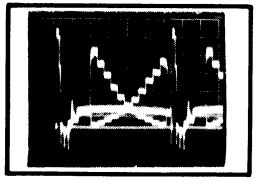
1 0.2V/DIV, 10μs/DIV



2 0.2V

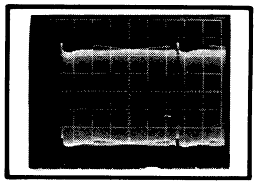


6 0.1V/DIV, 10μs/DIV



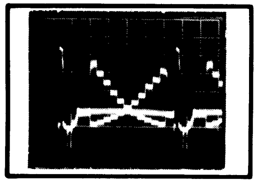
7 0.1V

11 0.2V/DIV 10μs/DIV



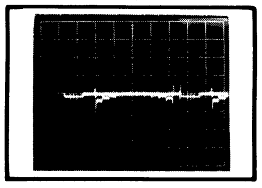
12 0.1

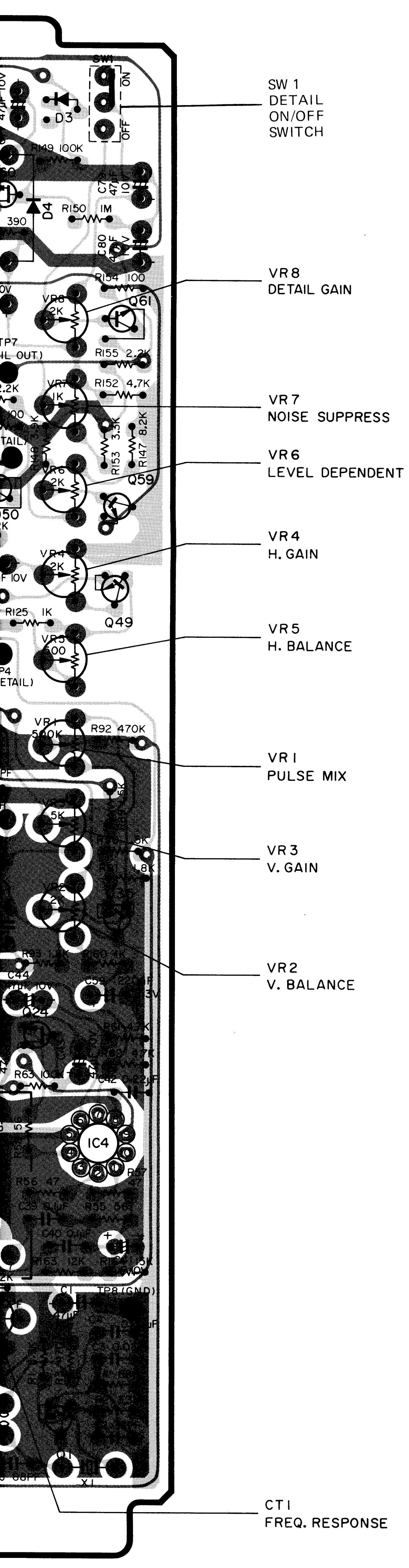
16 0.1V/DIV, 10μs/DIV



17 50n

21 0.2V/DIV, 10μs/DIV

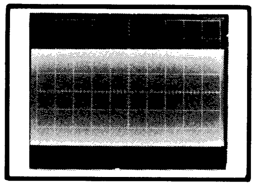



SW 1
DETAIL
ON/OFF
SWITCH
VR8
DETAIL GAIN
VR 7
NOISE SUPPRESS
VR 6
LEVEL DEPENDENT
VR 4
H. GAIN
VR 5
H. BALANCE
VR I
PULSE MIX
VR 3
V. GAIN
VR 2
V. BALANCE
CT I
FREQ. RESPONSE
SW1
ON
OFF
D3
D4
R149 100K
R150 1M
R154 100
R155 2.2K
R152 4.7K
R153 3.3K
R147 8.2K
Q61
Q59
Q49
R125 1K
R92 470K
IC4
TP7
TP8 (GND)
X1

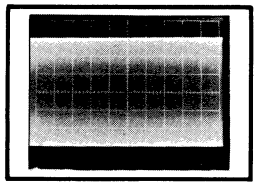
3

SIGNAL WAVEFORMS OF DETAIL BOARD

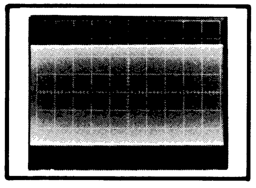
1 0.2V/DIV, 10μs/DIV



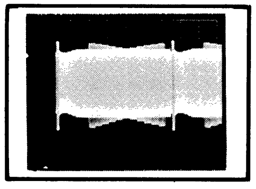
2 0.2V/DIV, 10μs/DIV



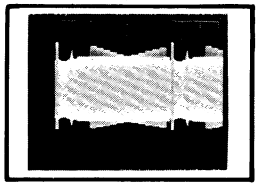
3 0.2V/DIV, 10μs/DIV



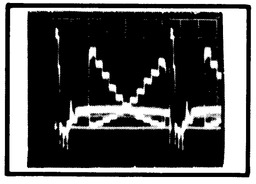
4 0.2V/DIV, 10μs/DIV



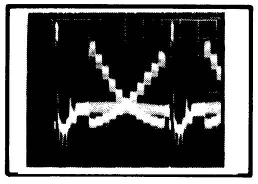
5 0.2V/DIV, 10μs/DIV



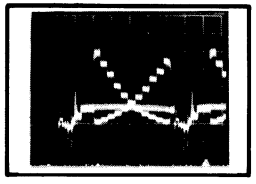
6 0.1V/DIV, 10μs/DIV



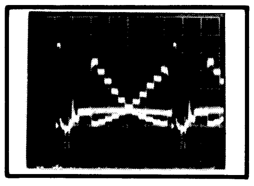
7 0.1V/DIV, 10μs/DIV



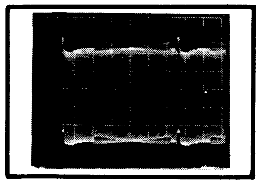
8 0.1V/DIV, 10μs/DIV



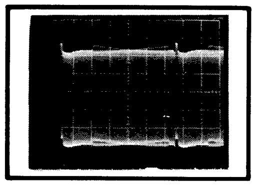
9 0.1V/DIV, 10μs/DIV



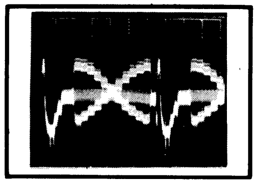
10 0.2V/DIV, 10μs/DIV



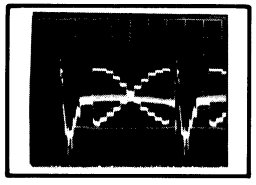
11 0.2V/DIV 10μs/DIV



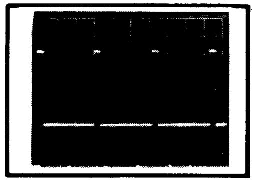
12 0.1V/DIV, 10μs/DIV



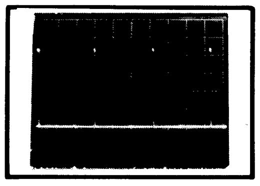
13 0.1V/DIV, 10μs/DIV



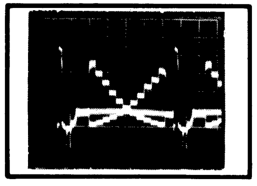
14 2V/DIV, 20μs/DIV



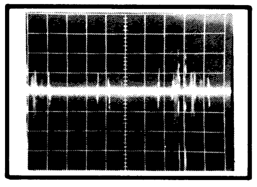
15 2V/DIV, 20μs/DIV



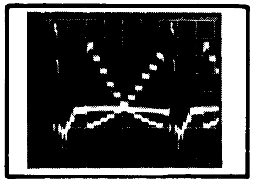
16 0.1V/DIV, 10μs/DIV



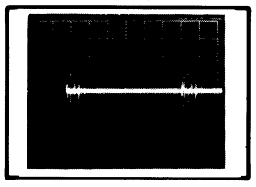
17 50mV/DIV, 2msec/DIV



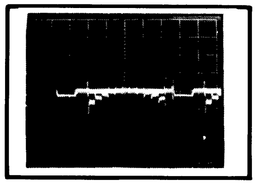
18 0.1V/DIV, 10μs/DIV



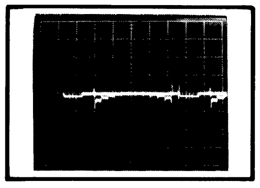
19 50mV/DIV, 10μs/DIV



20 0.2V/DIV, 10μs/DIV

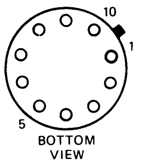


21 0.2V/DIV, 10μs/DIV

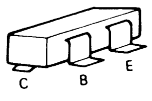


IC1	MC1496G		A3
IC2	YFMC1733CG		B2
IC3	YFTL062CPS		A2
IC4	YFMC1733CG		A3
Q1	2SC2404-CD	(U)	A3
Q2	2SC2480-S	(R)	A2
Q3	2SC2480-S	(R)	A2
Q4	2SC2480-S	(R)	A2
Q5	2SC2480-S	(R)	A2
Q6	2SA1022-CD	(E)	A2
Q7	2SK198-Q	(1O)	B2
Q8	2SA1022-CD	(E)	B2
Q9	2SA1022-CD	(E)	B2
Q10	2SC2405STU	(S)	B2
Q11	2SC641K-C		A2
Q12	2SK198-Q	(1O)	A2
Q13	2SC2405STU	(S)	A2
Q14	2SC641K-C		A2
Q15	2SA1022-CD	(E)	A2
Q16	2SA1022-CD	(E)	A2
Q17	2SC2295-BC	(V)	A2
Q19	2SC2480-S	(R)	B3
Q20	2SC2295-BC	(R)	A3
Q21	2SC2295-BC	(R)	A3
Q22	2SC2295-BC	(R)	A3
Q23	2SA1022-CD	(E)	A3
Q24	2SK198-Q	(1O)	B3
Q25	2SA1022-CD	(E)	B3
Q26	2SA1022-CD	(E)	B3
Q27	2SC2295-BC	(V)	B2
Q28	2SC2405STU	(S)	B3
Q29	2SC641K-C		A2
Q30	2SK198-Q	(1O)	A2
Q31	2SB709-QRS	(A)	B2
Q32	2SA1022-CD	(E)	B2
Q33	2SD601-QRS	(Y)	B2
Q34	2SD601-QRS	(Y)	A2
Q35	2SD601-QRS	(Y)	B3
Q36	2SD601-QRS	(Y)	B2
Q37	2SD601-QRS	(Y)	C2
Q38	2SB709-QRS	(A)	C2
Q39	2SC641K-C		C2
Q41	2SC641K-C		A2
Q42	2SK198-Q	(1O)	A2
Q43	2SC2405STU	(S)	C2
Q44	2SC2404-CD	(U)	B2
Q45	2SC2404-CD	(U)	B2
Q46	2SD601-QRS	(Y)	B2
Q47	2SB709-QRS	(A)	C2
Q48	2SD601-QRS	(Y)	C2
Q49	2SC2480-S	(R)	B3
Q50	2SD601-QRS	(Y)	C3
Q51	2SC2480-S	(R)	C2
Q52	2SC2405STU	(S)	C2
Q53	2SD661-STU		C2
Q54	2SB709-QRS	(A)	C2
Q55	2SD601-QRS	(Y)	C2
Q56	2SD601-QRS	(Y)	C3
Q57	2SK34-CD		C3
Q58	2SD601-QRS	(Y)	C3
Q59	2SD601-QRS	(Y)	C3
Q60	2SK198-Q	(1O)	C3
Q61	2SD601-QRS	(Y)	C3
Q62	2SD601-QRS	(Y)	B2
D1	MA151A	(MA)	B2
D2	MA151A	(MA)	B2
D3	MA151A	(MA)	C3
D4	1S1925		C3
D5	1S1925		C3
D6	MA151WA	(MT)	C2

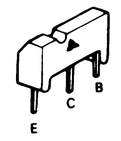
MC1496G
YFMC1733CG


10
1
5
BOTTOM
VIEW

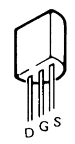
2SA1022-CD
2SB709-QRS
2SC2295-BC
2SC2404-CD
2SC2405STU
2SC2480-S
2SD601-QRS



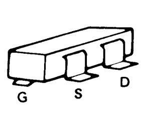
2SD661-STU



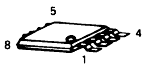
2SK34-CD



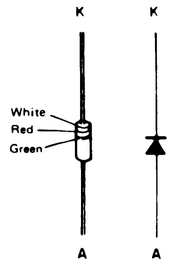
2SK198-Q



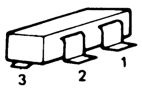
YFTL062CPS



1S1925

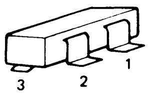

K
K
White
Red
Green
A
A

MA151WA



1 : Cathode
2 : Cathode
3 : Anode

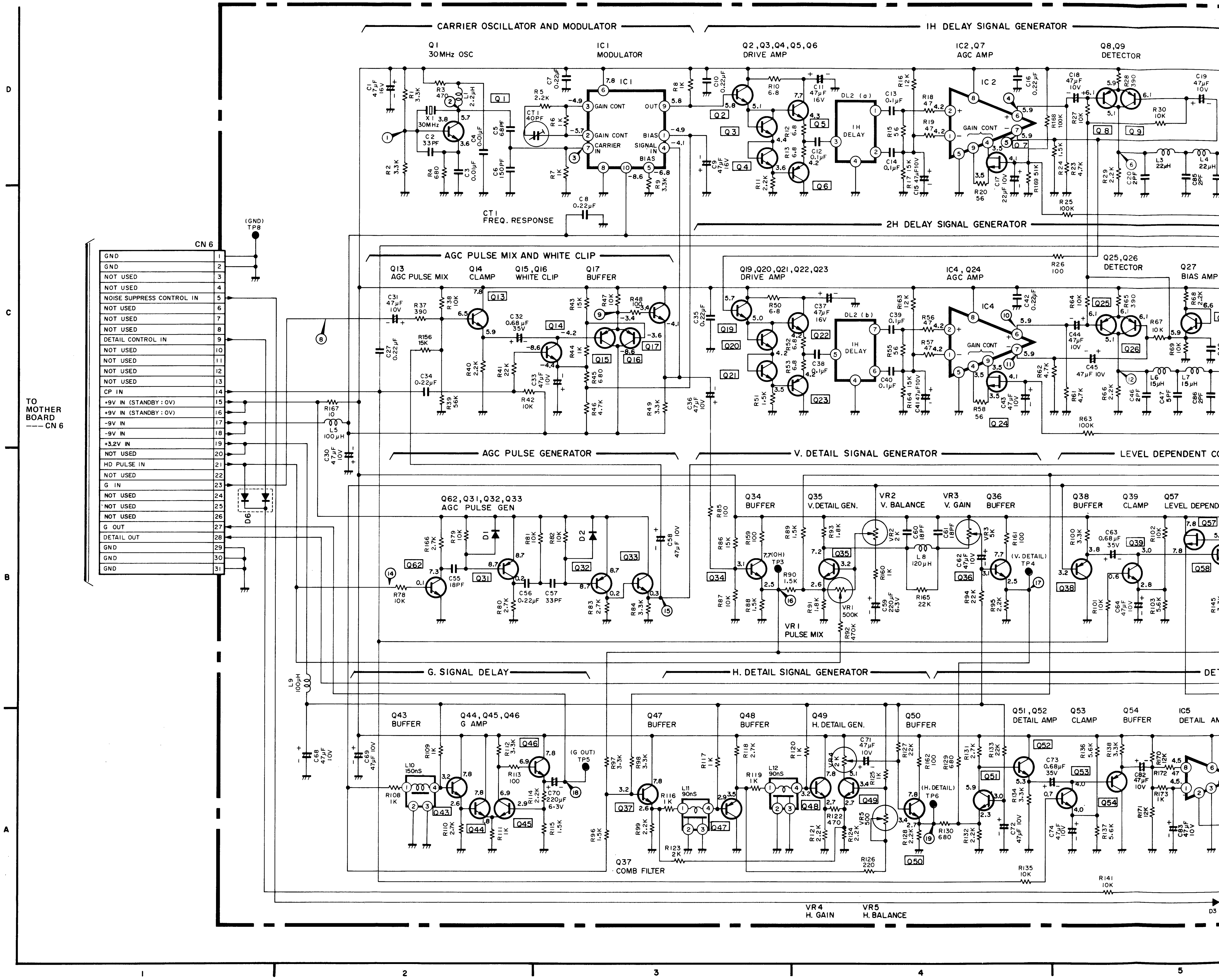
MA151A



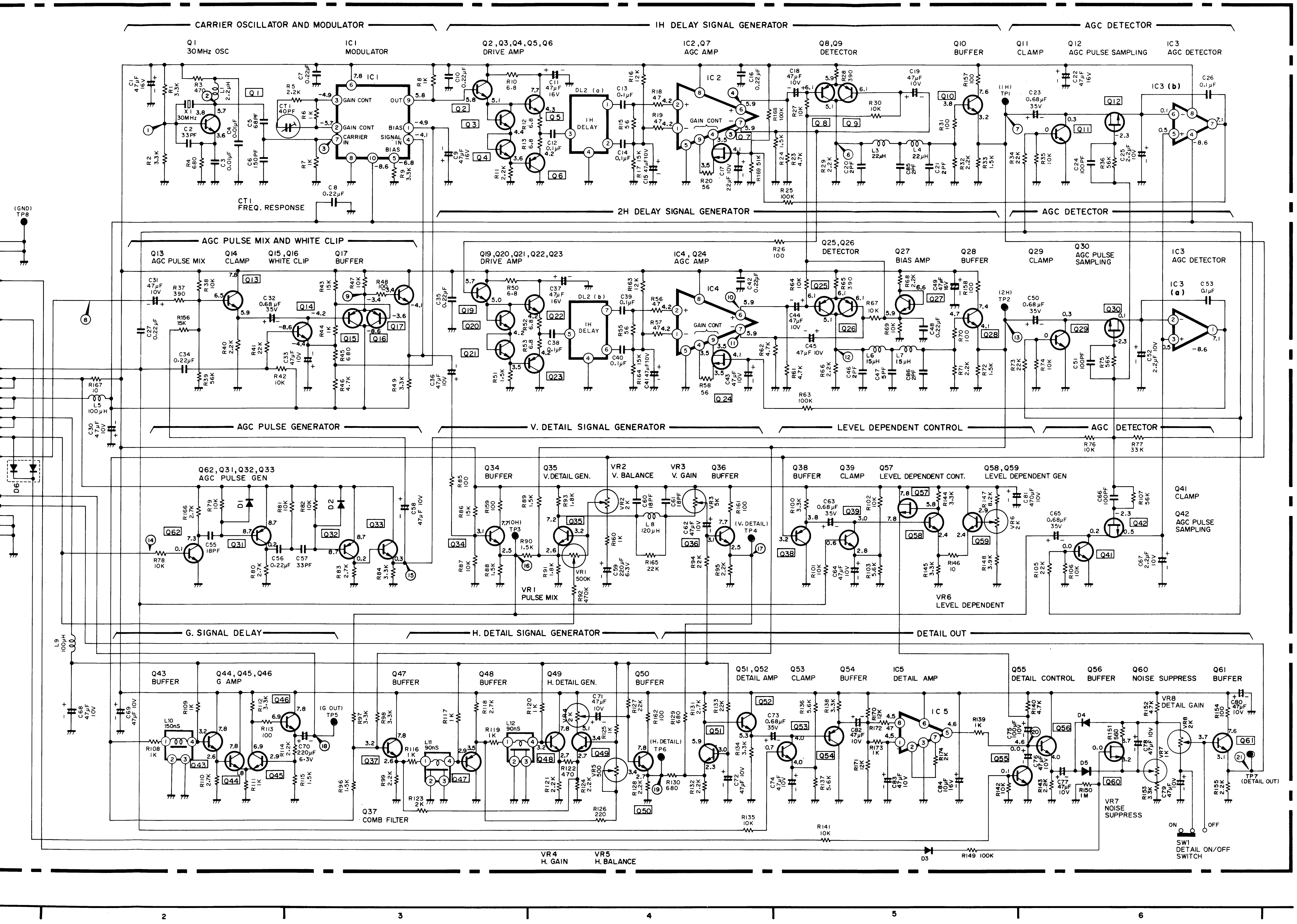
1 : NC
2 : Cathode
3 : Anode

IC1	MC1496G		D3
IC2	NE592K		D4
IC3	YFTL062CPS		C6, D6
IC4	NE592K		C4
IC5	NE592N8		A5
Q1	2SC2404-CD	(U)	D2
Q2	2SC2480-S	(R)	D3
Q3	2SC2480-S	(R)	D3
Q4	2SC2480-S	(R)	D3
Q5	2SC2480-S	(R)	D4
Q6	2SA1022-CD	(E)	D4
Q7	2SK198-Q	(1O)	D4
Q8	2SA1022-CD	(E)	D5
Q9	2SA1022-CD	(E)	D5
Q10	2SC2405STU	(S)	D5
Q11	2SC641K-C		D6
Q12	2SK198-Q	(1O)	D6
Q13	2SC2405STU	(S)	C2
Q14	2SC641K-C		C3
Q15	2SA1022-CD	(E)	C3
Q16	2SA1022-CD	(E)	C3
Q17	2SC2295-BC	(V)	C3
Q19	2SC2480-S	(R)	C3
Q20	2SC2480-S	(R)	C3
Q21	2SC2480-S	(R)	C3
Q22	2SC2480-S	(R)	C4
Q23	2SA1022-CD	(E)	C4
Q24	2SK198-Q	(1O)	C4
Q25	2SA1022-CD	(E)	C5
Q26	2SA1022-CD	(E)	C5
Q27	2SC2295-BC	(V)	C5
Q28	2SC2405STU	(S)	C5
Q29	2SC641K-C		C6
Q30	2SK198-Q	(1O)	C6
Q31	2SB709-QRS	(A)	B2
Q32	2SA1022-CD	(E)	B3
Q33	2SD601-QRS	(Y)	B3
Q34	2SD601-QRS	(Y)	B3
Q35	2SD601-QRS	(Y)	B4
Q36	2SD601-QRS	(Y)	B4
Q37	2SD601-QRS	(Y)	A3
Q38	2SB709-QRS	(A)	B5
Q39	2SC641K-C		B5
Q41	2SC641K-C		B6
Q42	2SK198-Q	(1O)	B6
Q43	2SC2405STU	(S)	A2
Q44	2SC2404-CD	(U)	A2
Q45	2SC2404-CD	(U)	A2
Q46	2SD601-QRS	(Y)	A3
Q47	2SB709-QRS	(A)	A3
Q48	2SD601-QRS	(Y)	A4
Q49	2SC2480-S	(R)	A4
Q50	2SD601-QRS	(Y)	A4
Q51	2SC2480-S	(R)	A4
Q52	2SC2405STU	(S)	A4
Q53	2SD661-STU		A5
Q54	2SB709-QRS	(A)	A5
Q55	2SD601-QRS	(Y)	A5
Q56	2SD601-QRS	(Y)	A5
Q57	2SK128-QR		B5
Q58	2SD601-QRS	(Y)	B5
Q59	2SD601-QRS	(Y)	B5
Q60	2SK198-Q	(1O)	A5
Q61	2SD601-QRS	(Y)	B2
Q62	2SD601-QRS	(Y)	B2
D1	MA151A	(MA)	B2
D2	MA151A	(MA)	B3
D3	MA151A	(MA)	A5
D4	1S1925		A5
D5	1S1925		A5
D6	MA151WK	(MT)	B1

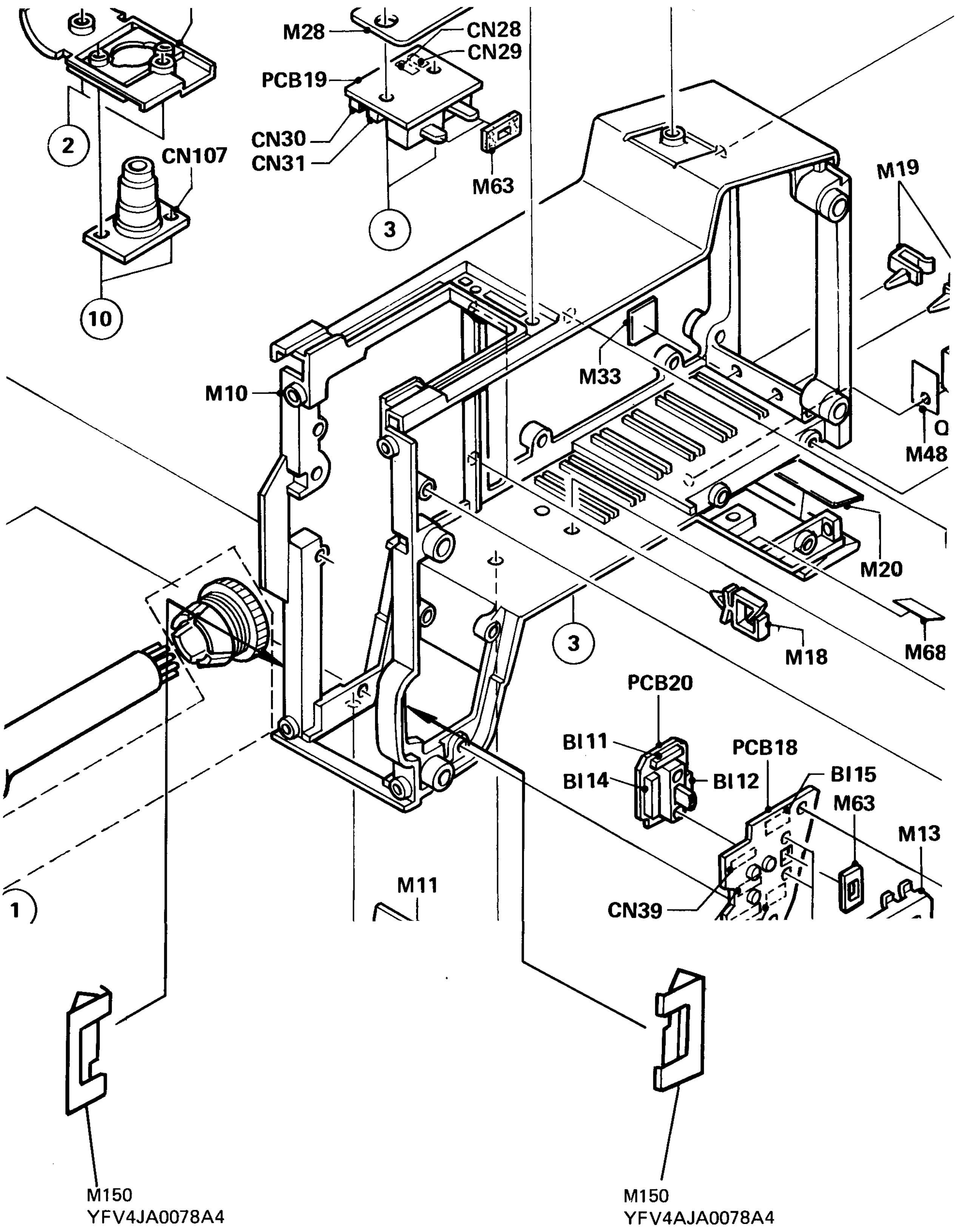
SCHEMATIC DIAGRAM OF DETAIL BOARD


CARRIER OSCILLATOR AND MODULATOR
Q1 30MHz OSC
IC1 MODULATOR
1H DELAY SIGNAL GENERATOR
Q2,Q3,Q4,Q5,Q6 DRIVE AMP
IC2,Q7 AGC AMP
Q8,Q9 DETECTOR
CT1 FREQ. RESPONSE
2H DELAY SIGNAL GENERATOR
AGC PULSE MIX AND WHITE CLIP
Q13 AGC PULSE MIX
Q14 CLAMP
Q15,Q16 WHITE CLIP
Q17 BUFFER
Q19,Q20,Q21,Q22,Q23 DRIVE AMP
IC4,Q24 AGC AMP
Q25,Q26 DETECTOR
Q27 BIAS AMP
AGC PULSE GENERATOR
Q62,Q31,Q32,Q33 AGC PULSE GEN
V. DETAIL SIGNAL GENERATOR
Q34 BUFFER
Q35 V.DETAIL GEN.
VR2 V. BALANCE
VR3 V. GAIN
Q36 BUFFER
VR1 PULSE MIX
LEVEL DEPENDENT CO
Q38 BUFFER
Q39 CLAMP
Q57 LEVEL DEPEND
G. SIGNAL DELAY
Q43 BUFFER
Q44,Q45,Q46 G AMP
(G OUT) TP5
H. DETAIL SIGNAL GENERATOR
Q47 BUFFER
Q48 BUFFER
Q49 H. DETAIL GEN.
Q50 BUFFER
Q37 COMB FILTER
(H. DETAIL) TP6
Q51,Q52 DETAIL AMP
Q53 CLAMP
Q54 BUFFER
IC5 DETAIL AM
DET
VR4 H. GAIN
VR5 H. BALANCE
1H DELAY
DL2 (a)
DL2 (b)
GAIN CONT
(GND) TP8
7.7(OH) TP3
(V. DETAIL) TP4
TO MOTHER BOARD ---CN6
CN6
GND 1
GND 2
NOT USED 3
NOT USED 4
NOISE SUPPRESS CONTROL IN 5
NOT USED 6
NOT USED 7
NOT USED 8
DETAIL CONTROL IN 9
NOT USED 10
NOT USED 11
NOT USED 12
NOT USED 13
CP IN 14
+9V IN (STANDBY: 0V) 15
+9V IN (STANDBY: 0V) 16
-9V IN 17
-9V IN 18
+3.2V IN 19
NOT USED 20
HD PULSE IN 21
NOT USED 22
G IN 23
NOT USED 24
NOT USED 25
NOT USED 26
G OUT 27
DETAIL OUT 28
GND 29
GND 30
GND 31
D6
D
C
B
A
1
2
3
4
5

SCHEMATIC DIAGRAM OF DETAIL BOARD


CARRIER OSCILLATOR AND MODULATOR
Q1 30MHz OSC
IC1 MODULATOR
CT1 FREQ. RESPONSE
1H DELAY SIGNAL GENERATOR
Q2,Q3,Q4,Q5,Q6 DRIVE AMP
IC2,Q7 AGC AMP
Q8,Q9 DETECTOR
Q10 BUFFER
AGC DETECTOR
Q11 CLAMP
Q12 AGC PULSE SAMPLING
IC3 AGC DETECTOR
2H DELAY SIGNAL GENERATOR
AGC PULSE MIX AND WHITE CLIP
Q13 AGC PULSE MIX
Q14 CLAMP
Q15,Q16 WHITE CLIP
Q17 BUFFER
Q19,Q20,Q21,Q22,Q23 DRIVE AMP
IC4,Q24 AGC AMP
Q25,Q26 DETECTOR
Q27 BIAS AMP
Q28 BUFFER
Q29 CLAMP
Q30 AGC PULSE SAMPLING
IC3 AGC DETECTOR
AGC PULSE GENERATOR
V. DETAIL SIGNAL GENERATOR
LEVEL DEPENDENT CONTROL
AGC DETECTOR
Q62,Q31,Q32,Q33 AGC PULSE GEN
Q34 BUFFER
Q35 V.DETAIL GEN.
VR2 V. BALANCE
VR3 V. GAIN
Q36 BUFFER
Q38 BUFFER
Q39 CLAMP
Q57 LEVEL DEPENDENT CONT.
Q58,Q59 LEVEL DEPENDENT GEN
Q41 CLAMP
Q42 AGC PULSE SAMPLING
VR1 PULSE MIX
VR6 LEVEL DEPENDENT
G. SIGNAL DELAY
H. DETAIL SIGNAL GENERATOR
DETAIL OUT
Q43 BUFFER
Q44,Q45,Q46 G AMP
Q47 BUFFER
Q48 BUFFER
Q49 H. DETAIL GEN.
Q50 BUFFER
Q51,Q52 DETAIL AMP
Q53 CLAMP
Q54 BUFFER
IC5 DETAIL AMP
Q55 DETAIL CONTROL
Q56 BUFFER
Q60 NOISE SUPPRESS
Q61 BUFFER
Q37 COMB FILTER
VR4 H. GAIN
VR5 H. BALANCE
VR7 NOISE SUPPRESS
VR8 DETAIL GAIN
SW1 DETAIL ON/OFF SWITCH
ON
OFF
(GND) TP8
(1H) TP1
(2H) TP2
7.7(0H) TP3
(V. DETAIL) TP4
(G OUT) TP5
(H. DETAIL) TP6
TP7 (DETAIL OUT)
D6
D3
R149 100K
2
3
4
5
6

4-8 Exploded View of Camera (WV-555)


M28
CN28
CN29
PCB19
CN30
CN31
M63
3
2
CN107
10
M19
M10
M33
Q
M48
M20
3
M18
M68
PCB20
BI11
PCB18
BI14
BI12
BI15
M63
M13
M11
CN39
1
M150
YFV4JA0078A4
M150
YFV4AJA0078A4

5. PARTS LIST

o The comparison for parts list of WV-555B Series is described in the Table 5-1.

PARTS LIST	WV-555	WV-555B
1. Camera	A	A
1-1 Miscellaneous	A	A, B
1-2 Optical Mechanism	A	A
1-3 Encoder Board	A, S4	A, S4
1-4 Mic Board	A, S3	A, S3
1-5 Pre-Preamplifier Board	A	A
1-6 Preamplifier Board for Red	A	A
1-7 Preamplifier Board for Green	A	A
1-8 Preamplifier Board for Blue	A	A
1-9 Mother Board	A, S3	A, S3, B
1-10 Process-1 Board	A, S4	A, S4
1-11 Process-2 Board	A, S4	A, S4, B
1-12 Sync Board	A, S3	A, S3, B
1-13 Detail Board	A	B
1-14 High Voltage AIC Board	A, S3	A, S3, B
1-15 Deflection Board	A	A, B
1-16 Auto Board	A or S1, S3	S1, S3, B
1-17 Power Board	A	A
1-18 Intercom Board	A	A
1-19 EVF Control Board	A	A
1-20 Centering Control Board	A	A
1-21 PIX Out Select Board	A	A
1-22 ACC—MAN Select Board	A	A
1-23 Accessory Parts/Packaging Parts	A	A, B
2. Zoom Lens (WV-LZ30/10)	A	A
3. 1.5" Viewfinder (WV-VF32)	A	A
4. Battery Pack (WV-PS37)	A	A
5. Tripod Mounting Adaptor (WV-Q37)	A	A
6. Battery Charger (WV-BC32)	A	A
7. VTR/STUDIO Extension VTR Cable	A	A
8. EXPLODED VIEW	A	A
8-1 Camera	A	A
8-2 Optical Mechanism	A	A
8-3 Zoom Lens	A	A
8-4 1.5" Viewfinder	A	A
8-5 Battery Pack	A	A
8-6 Tripod Mounting Adaptor	A	A
8-7 Battery Charger	A	A
8-8 VTR/STUDIO Extension VTR Cable	A	A
8-9 Packaging	A	A

A :	Original Service Manual for WV-555 (Order No. VKD83100784C8)
S1 :	Supplement-1 Service Manual for WV-555 (Order No. VKD84060842S8)
S3 :	Supplement-3 Service Manual for WV-555 (Order No. VKD84110883S8)
S4 :	Supplement-4 Service Manual for WV-555 (Order No. VKD85030901S8)
B :	Issued in this Service Manual for WV-555B

Table 5-1

5. REPLACEMENT PARTS LIST

SYMBOL NO.	ORIGINAL PARTS NO.	NEW PARTS NO.	DESCRIPTION
MISCELLANEOUS			
M20	–	**YFV7QA0606A4**	Main Label
M41	–	**YFV5ED0134A1**	Left Side Cover
M45	–	**YFV7SA0168AS**	Right Side Cover Assy
M150	–	**YFV4AJA0078A4**	Spacer
PCB 7 MOTHER BOARD			
C22	YF426102CHJ	**YF426222XM**	Ceramic 2200pF 50V
PCB 9 PROCESS-2 BOARD			
C9	ECEA1ASS470	**ECEA1AN470**	Electrolytic 47μF 10V
C16	ECEA1ASS470	**ECEA1AN470**	Electrolytic 47μF 10V
C43	–	**ECCF1H820JC**	Ceramic 82pF 50V
C44	–	**ECCF1H820JC**	Ceramic 82pF 50V
C45	–	**ECCF1H820JC**	Ceramic 82pF 50V
PCB 12 HIGH VOLTAGE AIC BOARD			
R61	ERJ8GCSJ222	**ERJ8GCSJ272**	Carbon 2.7K ohms 1/8W
R62	ERJ8GCSJ103	**ERJ8GCSJ822**	Carbon 8.2K ohms 1/8W
PCB 13 DEFLECTION BOARD			
IC1	NJM4556D	**NJM3415D**	IC
IC2	NJM4556D	**NJM3415D**	IC
IC3	NJM4556D	**NJM3415D**	IC
R23	ERD10TJ101	–	Deletion
R25	ERD10TJ101	–	Deletion
R27	ERD10TJ101	–	Deletion
R29	ERD10TJ101	–	Deletion
R31	ERD10TJ101	–	Deletion
R33	ERD10TJ101	–	Deletion
R40	ERD10TJ331	**ERD10TJ151**	Carbon 150 ohms 1/8W
C10	ECQP1102JZ	–	Deletion
C12	ECQP1102JZ	–	Deletion
C14	ECQP1102JZ	–	Deletion
C16	ECQP1102JZ	–	Deletion
C18	ECQP1102JZ	–	Deletion
C20	ECQP1102JZ	–	Deletion
PCB 14 AUTO BOARD			
IC14	80C4952GSK	**80C49242GS**	IC
R6	ERJ8GCSJ102	**ERJ8GCSG122**	Carbon 1.2K ohms 1/8W
R16	ERJ8GCSJ222	**ERJ8GCSJ272**	Carbon 2.7K ohms 1/8W
ACCESSORY PARTS/PACKAGING PARTS			
M113	YFV8RA0032BN	–	Deletion

SYM-BOL NO.	PART NO.	DESCRIPTION	
SYNC BOARD			
PCB009	YFVKZ555NE8A	Printed Circuit Board Assy	
IC1	SN74LS221S	IC	
IC2	TC40H002F	IC	
IC3	DN74LS05S	IC	
IC4	DN74LS09S	IC	
IC7	MP7260	IC	
IC8	TC4053BF	IC	
IC9	TC4050BF	IC	
IC10	TC40H002F	IC	
Q1-4	2SD601-QRS	Transistor	
Q5	2SB709-QRS	Transistor	
Q6	2SD601-QRS	Transistor	
Q8,9	2SD601-QRS	Transistor	
Q10	2SB709-QRS	Transistor	
Q11	2SD601-QRS	Transistor	
Q12	2SB709-QRS	Transistor	
Q13	2SD601-QRS	Transistor	
Q14	2SB709-QRS	Transistor	
Q15	2SD601-QRS	Transistor	
Q16	2SB709-QRS	Transistor	
Q17-20	2SD601-QRS	Transistor	
Q21	2SC641K-C	Transistor	
Q22	2SD601-QRS	Transistor	
Q23	2SB709-QRS	Transistor	
Q24	2SC641K-C	Transistor	
Q25	2SD601-QRS	Transistor	
D1	YUD1S2688	Diode	
D2	MA165	Diode	
D3	YUD1S2688	Diode	
D4	MA165	Diode	
D5	YUD1S2688	Diode	
R1,2	ERJ8GCSJ223	Carbon	22K ohms 1/8W
R3	ERJ8GCSG821	Carbon	820 ohms 1/8W
R4	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R5	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R6	ERJ8GCSJ331	Carbon	33 ohms 1/8W
R7	ERJ8GCSG272	Carbon	2.7K ohms 1/8W
R8	ERJ8GCSJ331	Carbon	330 ohms 1/8W
R9	ERJ8GCSG123	Carbon	12K ohms 1/8W
R10	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R11	ERJ8GCSJ152	Carbon	1.5K ohms 1/8W
R12	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R13	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R14	ERJ8GCSG332	Carbon	3.3K ohms 1/8W
R15	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R16	ERJ8GCSG123	Carbon	12K ohms 1/8W
R17	ERJ8GCSJ152	Carbon	1.5K ohms 1/8W
R18	ERJ8GCSJ561	Carbon	560 ohms 1/8W
R19	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R20	ERJ8GCSJ561	Carbon	560 ohms 1/8W
R21	ERJ8GCSG622	Carbon	6.2K ohms 1/8W
R22	ERJ8GCSJ104	Carbon	100K ohms 1/8W

SYM-BOL NO.	PART NO.	DESCRIPTION	
R25	ERJ8GCSG821	Carbon	820 ohms 1/8W
R26	ERJ8GCSG122	Carbon	1.2K ohms 1/8W
R27	ERJ8GCSG101	Carbon	100 ohms 1/8W
R28	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R29	ERJ8GCSG272	Carbon	2.7K ohms 1/8W
R31,32	ERJ8GCSJ223	Carbon	22K ohms 1/8W
R33	ERJ8GCSG391	Carbon	390 ohms 1/8W
R34	ERJ8GCSJ223	Carbon	22K ohms 1/8W
R35	ERJ8GCSG122	Carbon	1.2K ohms 1/8W
R36	ERJ8GCSJ223	Carbon	22K ohms 1/8W
R37-40	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R41,42	ERJ8GCSG101	Carbon	100 ohms 1/8W
R43	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R44,45	ERJ8GCSG101	Carbon	100 ohms 1/8W
R46	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R47,48	ERJ8GCSG101	Carbon	100 ohms 1/8W
R49	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R50-53	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R54	ERJ8GCSG273	Carbon	27K ohms 1/8W
R55	ERJ8GCSG102	Carbon	1K ohms 1/8W
R56	ERJ8GCSG911	Carbon	910 ohms 1/8W
R57	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R58	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R59	ERJ8GCSJ562	Carbon	5.6K ohms 1/8W
R60	ERJ8GCSG123	Carbon	12K ohms 1/8W
R61,62	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R63	ERJ8GCSJ182	Carbon	1.8K ohms 1/8W
R64,65	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R66,67	ERJ8GCSG333	Carbon	33K ohms 1/8W
R68	ERJ8GCSG332	Carbon	3.3K ohms 1/8W
R69,70	ERJ8GCSJ682	Carbon	6.8K ohms 1/8W
R71	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R72-74	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R75,76	ERJ8GCSG333	Carbon	33K ohms 1/8W
R77	ERJ8GCSG332	Carbon	3.3K ohms 1/8W
R81	ERJ8GCSJ472	Carbon	4.7K ohms 1/8W
R82	ERJ8GCSG821	Carbon	820 ohms 1/8W
R83	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R84	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R85,86	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R87	ERJ8GCSJ822	Carbon	8.2K ohms 1/8W
R88	ERJ8GCSJ182	Carbon	1.8K ohms 1/8W
R89	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R90	ERJ8GCSG101	Carbon	100 ohms 1/8W
R91	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R92	ERJ8GCSG101	Carbon	100 ohms 1/8W
R93	ERJ8GCSJ104	Carbon	100K ohms 1/8W
R94	ERJ8GCSG333	Carbon	33K ohms 1/8W
R95	ERJ8GCSG221	Carbon	220 ohms 1/8W
R98	ERJ8GCSG101	Carbon	100 ohms 1/8W
R99	ERJ8GCSJ104	Carbon	100K ohms 1/8W
R103,104	ERJ8GCSG333	Carbon	33K ohms 1/8W
R106	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R109	ERJ8GCSJ105	Carbon	1M ohms 1/8W
R110	ERJ8GCSG101	Carbon	100 ohms 1/8W
R111	ERJ8GCSJ152	Carbon	1.5K ohms 1/8W
R113	ERJ8GCSJ124	Carbon	120K ohms 1/8W

SYM-BOL NO.	PART NO.	DESCRIPTION	
R114	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R115	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R116,117	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R118	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
VR1	YFP0T3321S53	Variable Resistor	5K ohms
VR2	YFP0T3321S23	Variable Resistor	2K ohms
VR4,5	YFRG4HAX100K	Variable Resistor	100K ohms
C1,2	ECEA1ASS470	Electrolytic	47 µF 10V
C3	YF426681SLKS	Ceramic	680 pF 50V
C4	YF426151CHJS	Ceramic	150 pF 50V
C5	YF426103XMS	Ceramic	0.01µF 50V
C6	YF426222XKS	Ceramic	2200 pF 50V
C7	YF426103XMS	Ceramic	0.01µF 50V
C11	ECEA1ASS470	Electrolytic	47 µF 10V
C13	YF426101CHJS	Ceramic	100 pF 50V
C14,16	YF426100CHDS	Ceramic	10 pF 50V
C17	YF426060CHDS	Ceramic	6 pF 50V
C18	YF426104XKS	Ceramic	0.1 µF
C20	YF426101CHJS	Ceramic	100 pF 50V
C21	YF426103XMS	Ceramic	0.01µF 50V
C22	YF426270CHJS	Ceramic	27 pF 50V
C23	YF426330CHJS	Ceramic	33 pF 50V
C25,26	YF426103XMS	Ceramic	0.01µF 50V
C27	ECSF1CE106	Electrolytic	10 µF 16V
C28	YF426103XMS	Ceramic	0.01µF 50V
C29	YF426070CHDS	Ceramic	7 pF 50V
C30-32	YF426103XMS	Ceramic	0.01µF 50V
C33,34	ECSF1CE336	Electrolytic	33 µF 16V
C35	ECEA1HSS4R7	Electrolytic	4.7 µF 50V
C37	YF426221SLKS	Ceramic	220 pF 50V
C39,40	ECKY1H102WE	Ceramic	1000 pF 50V
C41	YF426330CHJS	Ceramic	33 pF 50V
C44	YF426221SLKS	Ceramic	220 pF 50V
C45	YF426102CHJS	Ceramic	1000 pF 50V
C46	ECEA1ASS470	Electrolytic	47 µF 10V
C47	YF426473XMS	Ceramic	0.047 µF 50V
C49	YF426470SLKS	Ceramic	47 pF 50V
C50	YF426330CHJS	Ceramic	33 pF 50V
C51	YF426102CHJS	Ceramic	1000 pF 50V
C52	YF426220CHKS	Ceramic	22 pF 50V
C53	YF426101CHJS	Ceramic	100 pF 50V
C54	YF426221SLKS	Ceramic	220 pF 50V
C55	YF426180CHJS	Ceramic	18 pF 50V
C57	YF426221SLKS	Ceramic	220 pF 50V
C58	YF426223XKS	Ceramic	0.022 µF 50V
C59	YF426103XMS	Ceramic	0.01µF 50V
C60	ECQP1222JZ	Plastic	2200 pF 100V
C61	YF426101CHJS	Ceramic	100 pF 50V
C62	ECSF1AE336	Electrolytic	33 µF 10V
C63	YF426222XKS	Ceramic	2200 pF 50V
C65	ECSF1CE336	Electrolytic	33 µF 16V
C66	ECSF1AE106	Electrolytic	10 µF 10V
C67	ECSF1AE336	Electrolytic	33 µF 10V
CT1-4	ECV1ZW25X53T	Trimmer Capacitor	25 pF

SYM-BOL NO.	PART NO.	DESCRIPTION	
L1	YFCSL094R7K	Coil	4.7 µH
L11,12	YFCSL09470K	Coil	47 µH
L13	YFCSL09-100K	Coil	10 µH
L15,16	YFCSL09470K	Coil	47 µH
SW1	YFKTP02	Special Switch	
X1,2	YFKD2034KDB	Crystal Oscillator	
X3	YFKD3246KAB	Crystal Oscillator	
CF1,2	YFSLC871-197	Filter	
J1-4	ERJ8GCS0R00	Jumper Resistor	
CN1	YFD531PTDS	Connector	
M114	YFV2HA0115B4	Shield Base	
M115	YFV2HB0116A4	Shield Cover	

DETAIL BOARD

PCB006	YFVKZ0555EDA	Printed Circuit Board Assy
IC1	MC1496G	IC
IC2	NE592K	IC
IC3	TL062CPS	IC
IC4	NE592K	IC
IC5	NE592N8	IC
Q1	2SC2404-CD	Transistor
Q2-5	2SC2480-S	Transistor
Q6	2SA1022-CD	Transistor
Q7	2SK198-Q	Transistor
Q8,9	2SA1022-CD	Transistor
Q10	2SC2405STU	Transistor
Q11	2SC641K-C	Transistor
Q12	2SK198-Q	Transistor
Q13	2SC2405STU	Transistor
Q14	2SC641K-C	Transistor
Q15,16	2SA1022-CD	Transistor
Q17	2SC2295-BC	Transistor
Q19-22	2SC2480-S	Transistor
Q23	2SA1022-CD	Transistor
Q24	2SK198-Q	Transistor
Q25,26	2SA1022-CD	Transistor
Q27	2SC2295-BC	Transistor
Q28	2SC2405STU	Transistor
Q29	2SC641K-C	Transistor
Q30	2SK198-Q	Transistor
Q31	2SB709-QRS	Transistor
Q32	2SA1022-CD	Transistor
Q33-37	2SD601-QRS	Transistor
Q38	2SB709-QRS	Transistor
Q39,41	2SC641K-C	Transistor
Q42	2SK198-Q	Transistor
Q43	2SC2405STU	Transistor
Q44,45	2SC2404-CD	Transistor
Q46	2SD601-QRS	Transistor
Q47	2SB709-QRS	Transistor
Q48	2SD601-QRS	Transistor
Q49	2SC2480-S	Transistor
Q50	2SD601-QRS	Transistor
Q51	2SC2480-S	Transistor
Q52	2SC2405STU	Transistor

SYM-BOL NO.	PART NO.	DESCRIPTION	
Q53	2SD661-STU	Transistor	
Q54	2SB709-QRS	Transistor	
Q55,56	2SD601-QRS	Transistor	
Q57	2SK128-QR	Transistor	
Q58,59	2SD601-QRS	Transistor	
Q60	2SK198-Q	Transistor	
Q61,62	2SD601-QRS	Transistor	
D1-3	MA151A	Diode	
D4,5	1S1925	Diode	
D6	MA151WK	Diode	
R1,2	ERJ8GCSJ332	Carbon	3.3K ohms 1/8W
R3	ERJ8GCSJ471	Carbon	470 ohms 1/8W
R4	ERJ8GCSJ681	Carbon	680 ohms 1/8W
R5	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R6-8	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R9	ERJ8GCSJ332	Carbon	3.3K ohms 1/8W
R10	ERJ8GCSK6R8	Carbon	6.8 ohms 1/8W
R11	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R12,13	ERJ8GCSK6R8	Carbon	6.8 ohms 1/8W
R15	ERJ8GCSJ560	Carbon	56 ohms 1/8W
R16	ERJ8GCSJ123	Carbon	12K ohms 1/8W
R17	ERJ8GCSJ153	Carbon	15K ohms 1/8W
R18,19	ERJ8GCSJ470	Carbon	47 ohms 1/8W
R20	ERJ8GCSJ560	Carbon	56 ohms 1/8W
R23	ERJ8GCSJ472	Carbon	4.7K ohms 1/8W
R24	ERJ8GCSJ152	Carbon	1.5K ohms 1/8W
R25	ERJ8GCSJ104	Carbon	100K ohms 1/8W
R26	ERJ8GCSJ101	Carbon	100 ohms 1/8W
R27	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R28	ERJ8GCSJ391	Carbon	390 ohms 1/8W
R29	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R30	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R31	ERJ8GCSJ101	Carbon	100 ohms 1/8W
R32	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R33	ERJ8GCSJ152	Carbon	1.5K ohms 1/8W
R34	ERJ8GCSJ223	Carbon	22K ohms 1/8W
R35	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R36	ERJ8GCSJ563	Carbon	56K ohms 1/8W
R37	ERJ8GCSJ391	Carbon	390 ohms 1/8W
R38	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R39	ERJ8GCSJ563	Carbon	56K ohms 1/8W
R40	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R41	ERJ8GCSJ223	Carbon	22K ohms 1/8W
R42	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R43	ERJ8GCSJ153	Carbon	15K ohms 1/8W
R44	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R45	ERJ8GCSJ681	Carbon	680 ohms 1/8W
R46	ERJ8GCSJ472	Carbon	4.7K ohms 1/8W
R47	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R48	ERJ8GCSJ101	Carbon	100 ohms 1/8W
R49	ERJ8GCSJ332	Carbon	3.3K ohms 1/8W
R50	ERJ8GCSK6R8	Carbon	6.8 ohms 1/8W
R51	ERJ8GCSJ152	Carbon	1.5K ohms 1/8W
R52,53	ERJ8GCSK6R8	Carbon	6.8 ohms 1/8W
R55	ERJ8GCSJ560	Carbon	56 ohms 1/8W

SYM-BOL NO.	PART NO.	DESCRIPTION	
R56,57	ERJ8GCSJ470	Carbon	47 ohms 1/8W
R58	ERJ8GCSJ560	Carbon	56 ohms 1/8W
R61,62	ERJ8GCSJ472	Carbon	4.7K ohms 1/8W
R63	ERJ8GCSJ104	Carbon	100K ohms 1/8W
R64	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R65	ERJ8GCSJ391	Carbon	390 ohms 1/8W
R66	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R67	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R68	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R69	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R70	ERJ8GCSJ101	Carbon	100 ohms 1/8W
R71	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R72	ERJ8GCSJ152	Carbon	1.5K ohms 1/8W
R73	ERJ8GCSJ223	Carbon	22K ohms 1/8W
R74	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R75	ERJ8GCSJ563	Carbon	56K ohms 1/8W
R76	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R77	ERJ8GCSJ333	Carbon	33K ohms 1/8W
R78,79	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R80	ERJ8GCSJ272	Carbon	2.7K ohms 1/8W
R81,82	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R83	ERJ8GCSJ272	Carbon	2.7K ohms 1/8W
R84	ERJ8GCSJ332	Carbon	3.3K ohms 1/8W
R85	ERJ8GCSJ101	Carbon	100 ohms 1/8W
R86	ERJ8GCSJ153	Carbon	15K ohms 1/8W
R87	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R88	ERJ8GCSJ152	Carbon	1.5K ohms 1/8W
R89,90	ERJ8GCSG152	Carbon	1.5K ohms 1/8W
R91	ERJ8GCSJ182	Carbon	1.8K ohms 1/8W
R92	ERJ8GCSJ474	Carbon	470K ohms 1/8W
R93	ERJ8GCSJ182	Carbon	1.8K ohms 1/8W
R94	ERJ8GCSJ223	Carbon	22K ohms 1/8W
R95	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R96	ERJ8GCSJ152	Carbon	1.5K ohms 1/8W
R97,98	ERJ8GCSJ332	Carbon	3.3K ohms 1/8W
R99	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R100	ERJ8GCSJ332	Carbon	3.3K ohms 1/8W
R101,102	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R103	ERJ8GCSJ562	Carbon	5.6K ohms 1/8W
R105	ERJ8GCSJ223	Carbon	22K ohms 1/8W
R106	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R107	ERJ8GCSJ563	Carbon	56K ohms 1/8W
R108,109	ERJ8GCSG102	Carbon	1K ohms 1/8W
R110	ERJ8GCSJ272	Carbon	2.7K ohms 1/8W
R111	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R112	ERJ8GCSJ332	Carbon	3.3K ohms 1/8W
R113	ERJ8GCSJ101	Carbon	100 ohms 1/8W
R114	ERJ8GCSG222	Carbon	2.2K ohms 1/8W
R115	ERJ8GCSG152	Carbon	1.5K ohms 1/8W
R116,117	ERJ8GCSG102	Carbon	1K ohms 1/8W
R118	ERJ8GCSJ272	Carbon	2.7K ohms 1/8W
R119,120	ERJ8GCSG102	Carbon	1K ohms 1/8W
R121	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R122	ERJ8GCSJ471	Carbon	470 ohms 1/8W
R123	ERJ8GCSG202	Carbon	2K ohms 1/8W

SYMBOL NO.	PART NO.	DESCRIPTION	
R124	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R125	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R126	ERJ8GCSJ221	Carbon	220 ohms 1/8W
R127	ERJ8GCSJ223	Carbon	22K ohms 1/8W
R128	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R129,130	ERJ8GCSJ681	Carbon	680 ohms 1/8W
R131	ERJ8GCSJ272	Carbon	2.7K ohms 1/8W
R132	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R133	ERJ8GCSJ223	Carbon	22K ohms 1/8W
R134	ERJ8GCSJ332	Carbon	3.3K ohms 1/8W
R135	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R136,137	ERJ8GCSJ562	Carbon	5.6K ohms 1/8W
R138	ERJ8GCSJ332	Carbon	3.3K ohms 1/8W
R139	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R140	ERJ8GCSJ472	Carbon	4.7K ohms 1/8W
R141,142	ERJ8GCSJ103	Carbon	10K ohms 1/8W
R143	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R144,145	ERJ8GCSJ332	Carbon	3.3K ohms 1/8W
R146	ERJ8GCSJ100	Carbon	10 ohms 1/8W
R147	ERJ8GCSJ822	Carbon	8.2K ohms 1/8W
R148	ERJ8GCSJ392	Carbon	3.9K ohms 1/8W
R149	ERJ8GCSJ104	Carbon	100K ohms 1/8W
R150	ERJ8GCSJ105	Carbon	1M ohms 1/8W
R151	ERJ8GCSJ561	Carbon	560 ohms 1/8W
R152	ERJ8GCSJ472	Carbon	4.7K ohms 1/8W
R153	ERJ8GCSJ332	Carbon	3.3K ohms 1/8W
R154	ERJ8GCSJ101	Carbon	100 ohms 1/8W
R155	ERJ8GCSJ222	Carbon	2.2K ohms 1/8W
R156	ERJ8GCSJ153	Carbon	15K ohms 1/8W
R157-159	ERJ8GCSJ101	Carbon	100 ohms 1/8W
R160	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R161,162	ERJ8GCSJ101	Carbon	100 ohms 1/8W
R163	ERJ8GCSJ123	Carbon	12K ohms 1/8W
R164	ERJ8GCSJ153	Carbon	15K ohms 1/8W
R165	ERJ8GCSJ223	Carbon	22K ohms 1/8W
R166	ERJ8GCSJ272	Carbon	2.7K ohms 1/8W
R167	ERD25FJ100	Carbon	10 ohms 1/4W
R168	ERJ8GCSJ104	Carbon	100K ohms 1/8W
R169	ERJ8GCSJ513	Carbon	51K ohms 1/8W
R170,171	ERJ8GCSJ123	Carbon	12K ohms 1/8W
R172	ERJ8GCSJ470	Carbon	47 ohms 1/8W
R173	ERJ8GCSJ102	Carbon	1K ohms 1/8W
R174	ERJ8GCSJ202	Carbon	2K ohms 1/8W
VR1	YFP0T3321S55	Variable Resistor	500K ohms
VR2	YFP0T3321S23	Variable Resistor	2K ohms
VR3	YFP0T3321S53	Variable Resistor	5K ohms
VR4	YFP0T3321S23	Variable Resistor	2K ohms
VR5	YFP0T3321S52	Variable Resistor	500 ohms
VR6	YFP0T3321S23	Variable Resistor	2K ohms
VR7	YFP0T3321S13	Variable Resistor	1K ohms
VR8	YFP0T3321S23	Variable Resistor	2K ohms
C1	ECSF1CE476	Electrolytic	47 µF 16V
C2	YF426330CHJS	Ceramic	33 pF 50V
C3,4	YF426103XMS	Ceramic	0.01 µF 50V
C5	YF426680CHJS	Ceramic	68 pF 50V
C6	YF426151CHJS	Ceramic	150 pF 50V
C7,8	YF426224FZS	Ceramic	0.22 µF 50V
C9	ECSF1CE476	Electrolytic	47 µF 16V
C10	YF426224FZS	Ceramic	0.22 µF 50V

SYMBOL NO.	PART NO.	DESCRIPTION	
C11	ECSF1CE476	Electrolytic	47 µF 16V
C12-14	YF426104DMS	Ceramic	0.1 µF 50V
C15	ECEA1ASS470	Electrolytic	47µF 10V
C16	YF426224FZS	Ceramic	0.22 µF 50V
C17	ECEA1ASS220	Electrolytic	22 µF 10V
C18,19	ECEA1ASS470	Electrolytic	47 µF 10V
C20,21	YF426020CHDS	Ceramic	2pF 50V
C22	ECSF1CE476	Electrolytic	47 µF 16V
C23	ECSF35ER68	Electrolytic	0.68 µF 35V
C24	YF426101CHJS	Ceramic	100 pF 50V
C25	ECSF10E2R2	Electrolytic	2.2 µF 10V
C26	YF426104DMS	Ceramic	0.1 µF 50V
C27	YF426224FZS	Ceramic	0.22 µF 50V
C30,31	ECEA1ASS470	Electrolytic	47 µF 10V
C32	ECSF35ER68	Electrolytic	0.68 µF 35V
C33	ECEA1ASS470	Electrolytic	47 µF 10V
C34,35	YF426224FZS	Ceramic	0.22 µF 50V
C36	ECEA1ASS470	Electrolytic	47 µF 10V
C37	ECSF1CE476	Electrolytic	47 µF 16V
C38-40	YF426104DMS	Ceramic	0.1 µF 50V
C41	ECEA1ASS470	Electrolytic	47µF 10V
C42	YF426224FZS	Ceramic	0.22 µF 50V
C43-45	ECEA1ASS470	Electrolytic	47 µF 10V
C46	YF426020CHDS	Ceramic	2 pF 50V
C47	YF426050CHDS	Ceramic	5 pF 50V
C48	YF426224FZS	Ceramic	0.22 µF 50V
C49	ECSF1CE476	Electrolytic	47 µF 16V
C50	ECSF35ER68	Electrolytic	0.68 µF 35V
C51	YF426101CHJS	Ceramic	100 pF 50V
C52	ECSF10E2R2	Electrolytic	2.2 µF 10V
C53	YF426104DMS	Ceramic	0.1 µF 50V
C55	YF426180CHJS	Ceramic	18 pF 50V
C56	YF426224FZS	Ceramic	0.22 µF 50V
C57	YF426330CHJS	Ceramic	33 pF 50V
C58	ECEA1ASS470	Electrolytic	47 µF 10V
C59	ECEA0JSS221	Electrolytic	220 µF 6.3V
C60,61	YF426180CHJS	Ceramic	18 pF 50V
C62	ECEA1ASS470	Electrolytic	47 µF 10V
C63	ECSF35ER68	Electrolytic	0.68 µF 35V
C64	ECEA1ASS470	Electrolytic	47 µF 10V
C65	ECSF35ER68	Electrolytic	0.68 µF 35V
C66	YF426101CHJS	Ceramic	100 pF 50V
C67	ECSF10E2R2	Electrolytic	2.2 µF 10V
C68,69	ECEA1ASS470	Electrolytic	47 µF 10V
C70	ECEA0JSS221	Electrolytic	220 µF 6.3V
C71,72	ECEA1ASS470	Electrolytic	47 µF 10V
C73	ECSF35ER68	Electrolytic	0.68 µF 35V
C74	ECEA1ASS470	Electrolytic	47 µF 10V
C75	ECEA1ASS101	Electrolytic	100 µF 10V
C76-80	ESEA1ASS470	Electrolytic	47µF 10 V
C81	ECEA1ASS471	Electrolytic	470µF 10V
C82,83	ECEA1ASS470	Electrolytic	47 µF 10V
C84	ECSF1CE106	Electrolytic	10µF 16V
C85,86	ECCF1H020CC	Ceramic	2 pF 50V
CT1	ECV1ZW40X53T	Trimmer Capacitor	40 pF
L1	YWL52R2J	Coil	2.2 µH
L3,4	YWL5220J	Coil	22 µH
L5	EL05SI101K	Coil	100 µH
L6,7	YWL5150J	Coil	15 µH

SYMBOL NO.	PART NO.	DESCRIPTION	
L8	YFLS7121J	Coil	120 μH
L9	EL05SI101K	Coil	100 μH
L10	YFDL102A1506	Delay Line	150 nS
L11,12	YFDL102A9007	Delay Line	90 nS
DL2	EFDND645H06C	Delay Line	2H
SW1	YFSSS212YK	Slide Switch	
X1	YFKD2175KCC	Crystal-Oscillator	30 MHz
J1	ERJ8GCSJ0R00	Jumper Resistor	
CN1	YFD531PTDS	Multi-pin Connector	

Printed in Japan
B–370 4

ORDER NO. VKD84060842S8

Service Manual

Vol. 1

Circuit Description

Colour Video Camera

WV-555 Series

Supplement-1

Panasonic
WV-555
Panasonic

- The automatic centering control circuit on the Auto board has been changed to improve the function of automatic centering control from serial No. 41A00001 and higher.
- Please file this supplement service manual with the service manual order No. VKD83100784C8.

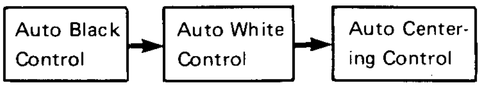
Panasonic

Matsushita Electric Trading Co., Ltd.
P.O. Box 288, Central Osaka Japan

7. Auto Board

7-1 Auto Black Control (ABC) Circuit 1
7-2 Auto white Control Circuit ...,......................... 3
7-3 Auto Centerring Control Circuit 5

It is recommended that the auto control are set in the following sequence as;



7-1 Auto Black Control (ABC) Circuit

Outline

This circuit automatically makes the pedestal levels of the red (R) and the blue (B) image match with the pedestal level of the green (G) image by utilizing the analog switches, comparator and microprocessor which instructs the change of the pedestal level for the red (R) and the blue (B) images.

When the pedestal levels of R signal and B signal become same as the pedestal level of G signal, the black balance is set and the microprocessor memorizes the black balance for long period of the time until next black balance is set.

Details

When the Auto White/Auto Black Set Switch on the front of the camera is pressed down to ABC position for the automatic black balance setting, the iris of the power servo control zoom lens is automatically closed for blocking the incoming light and the black balance is set automatically in approximately 5 seconds. After completing the black balance setting, the lens iris is automatically returned to the previous position.

If the black balance must be set in the manual iris control mode, the incoming light should be blocked by closing the lens iris manually, setting the filter wheel of the camera to No. 4 (CLOSE) or capping the lens.

The ABC start pulse is fed to the pin 14 of the IC15 through the input interface IC16(b), pin 4 of CN4 on this board (also pin 4 of CN4 on the mother board), C4 and pin 2 of BI1 on the mother board, pin 2 of CN39 and pin 5 of CN41 on the centering control board as starting of the auto black control circuit.

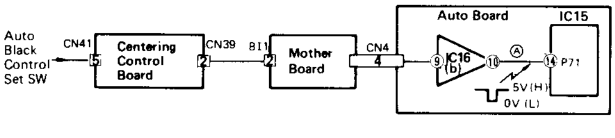


Fig. 7-1-1

The R, B, G signals are fed from pin 3/5/7 of the CN4 to the buffer Q1/Q2/Q3 respectively and are clamped by Q4/Q5/Q6 respectively.

The clamp level is set to 4.5V. The fine adjustment of the clamp level for R and B signal are taken by VR7 for R signal and VR8 for B signal and matched with G signal. The analog switcher IC6 is controlled by AWC busy pulse which is low (L) level when the auto black control is setting so that the analog switcher IC6 is set to L position for the auto black control.

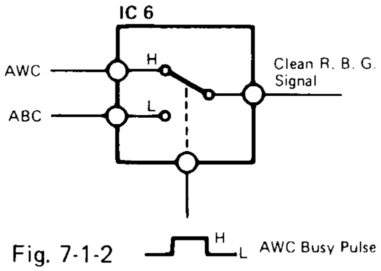


Fig. 7-1-2

The clamped R, B and G signals are respectively fed to pin 12, pin 5 and pin 2 of the analog switcher IC7 which are switched by the positive polarity vertical blanking pulse from pin 22 of CN4.

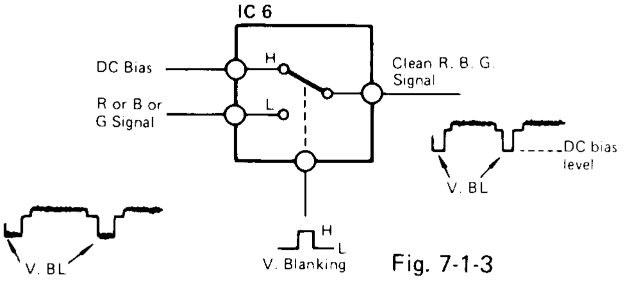


Fig. 7-1-3

The DC bias level is lower than the clamping level and noise on the vertical blanking is eliminated by analog switcher IC7 which flows DC bias during vertical blanking.

The clean R signal is fed to pin 1 of IC10(a) from pin 14 of IC7(a) and the clean B signal is fed to pin 2 of IC10(a) from pin 4 of IC7(b) and the clean G signal is fed to pin 5 of IC10(c) from pin 15 of IC7(c).

The analog switcher IC10(a) is controlled by the B/R selection pulse at pin 10 of IC10(a) from pin 20 of IC15 through the inverter Q10 so that the B signal is selected when the B/R selection pulse at pin 10 of IC10(a) is low (L) and the R signal is selected when the B/R selection pulse at pin 10 of IC10(a) is high (H). The analog switcher IC10(c) is controlled by the pulse at pin 9 of IC10(c) from pin 19 of IC15 through the inverter Q11 so that the G signal is selected when the pulse at pin 9 of IC10(c) is low (L) and B or R signal is selected when the pulse at pin 9 of IC10(c) is high(H). Therefore, B or R or G signal is fed to pin 10 of the operating amplifier IC11(c) from pin 4 of IC10(c).

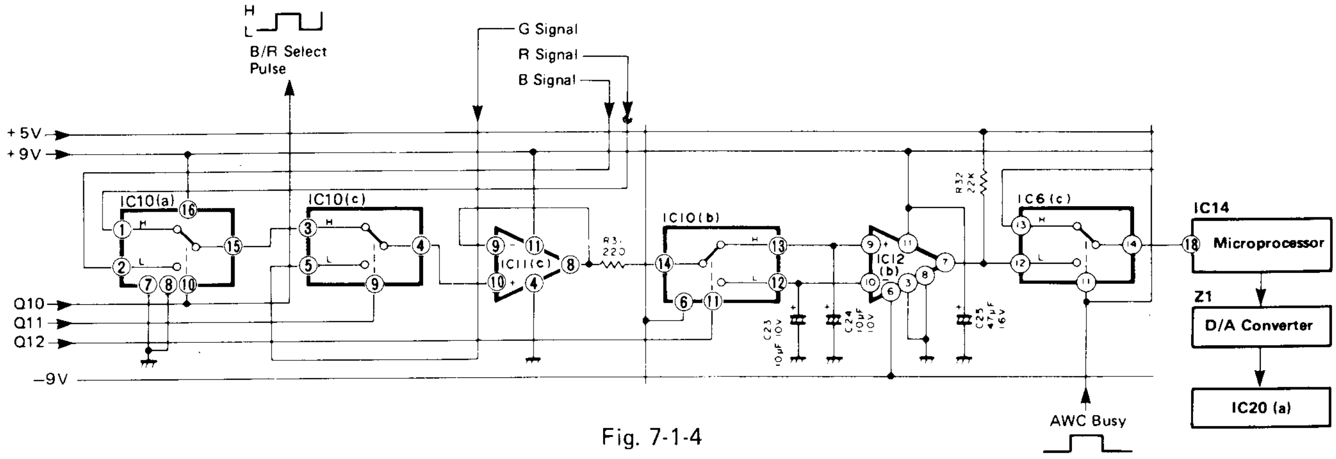

H
L
B/R Select Pulse
G Signal
R Signal
B Signal
+5V
+9V
Q10
Q11
Q12
−9V
IC10(a)
IC10(c)
IC11(c)
R31 220
IC10(b)
IC12 (b)
C23 10μF 10V
C24 10μF 10V
R32 22K
C25 47μF 16V
IC6(c)
IC14
Microprocessor
Z1
D/A Converter
IC20 (a)
AWC Busy

Fig. 7-1-4

The B or R or G signal are integrated by the integrator R31 and C23 or C24 for converting DC level.
The analog switchers IC10(a), IC10(c), IC10(b) are controlled by the pulses from pin 20/19/18 of IC15 respectively as;

(1) IC10(c) is set to L position and then IC10(b) is set to L position for integrating G signal to DC level by R31 and C23 and fed to pin 10 of the comparator IC12(b).

(2) IC10(b) is switched to H position after G signal is integrated to DC level and then IC10(c) is switched to H position for B and R signals.

(3) IC10(a) is set to L position for B signal so that B signal is integrated to DC level by R31 and C24 and fed to pin 9 of IC12(b), or IC10(a) is set to H position for R signal so that R signal is integrated to DC level by R31 and C24 and fed to pin 9 of IC12(b).

The IC6(c) is set to L position for ABC function so that the high (H) or low (L) at pin 7 of IC12(b) is fed to pin 18 of the microprocessor IC14.

If the DC level of B or R signal is higher than DC level of G signal, the output of the comparator IC12(b) shows high (H) so that the microprocessor IC14 instructs the count down 8-bit digital code to D/A converter Z1 and the analog level at pin 10 of Z1 is fed to the buffer IC20(a).
The analog level at pin 1 of IC20(a) is fed to pin 3 of the analog switchers IC18 and IC19 which switch position is selected by the signal at pin 9/10/11 of IC18 and IC19. The pin 1 of IC18 and IC19 are fed to pin 10 of IC21(c) for R pedestal and pin 5 of IC22(b) for B pedestal respectively. The signal at IC18 and IC19 are controlled by inhibit signal at pin 6 of IC18 and IC19.

The analog level for countdown is fed to IC21(c) for reducing R pedestal level or fed to IC22(b) for reducing B pedestal level until DC level of R-G and B-G signal becomes minimum.
If the DC level of B or R signal is lower than DC level of G signal, the output of the comparator IC12(b) shows low (L) so that the microprocessor IC14 instructs the 8-bit countup digital code to D/A converter Z1 and the analog level at pin 10 of Z1 is fed to buffer IC20(a).

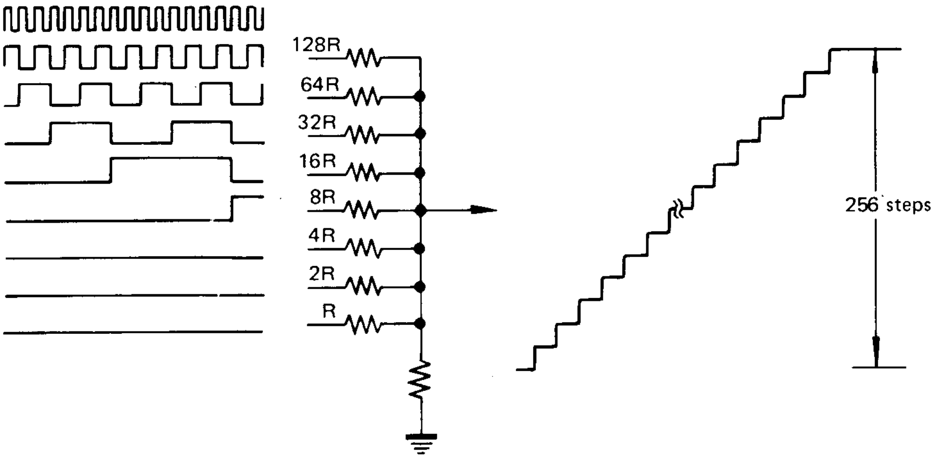

128R
64R
32R
16R
8R
4R
2R
R
256 steps

Fig. 7-1-5 ·D/A Converter Z1

The analog level for countup is fed to IC21(c) for increasing R pedestal level or fed to IC22(b) for increasing B pedestal level until DC level of R-G and B-G signal becomes minimum.

As a result, the B and R pedestal level match the G pedestal level automatically and the black balance setting is accomplished.

7-2 Auto White Control (AWC) Circuit

Outline

This circuit is automatically made the peak level of the red (R) and blue (B) image for matching them with the peak level of the green (G) image by utilizing the analog switches, comparator and microprocessor which instructs the change of the red (R) gain and the blue (B) gain.

When the R signal and B signal levels become same as the G signal level, the white balance is set and the microprocessor memorizes the white balance for long period of time until next white balance is set.

Details

When the Auto White/Auto Black Set Switch on the front of the camera is pressed up to AWC position for the automatic white balance setting while aiming the camera at a white object, the AWC start pulse is fed to the pin 13 of the IC15 through the input interface IC16(a), pin 2 of CN4 on this board (also pin 2 of CN4 on the mother board), C2 and pin 1 of BI1 on the mother board, pin 1 of CN39 and pin 4 of CN41 on the centering control board as starting of the auto white control circuit.

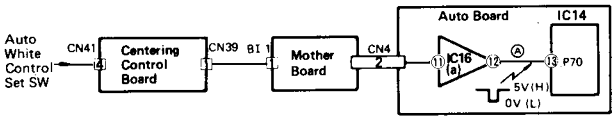


Fig. 7-2-1

The AWC busy pulse (positive polarity) from pin 11 of the microprocessor IC14 selects the analog switch IC6 to high (H) position for the auto white control.

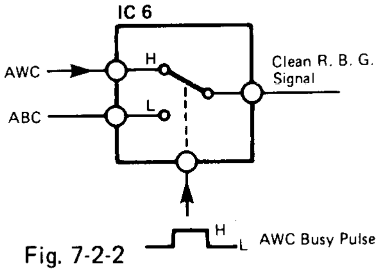


Fig. 7-2-2

The chroma signals R, B and G are respectively clamped by Q4, Q5 and Q6 and the clamp level is set to 4.5V. The fine adjustment of the clamp level for R and B signal are taken by VR5 for R signal and VR6 for B signal and matched with G signal.

The clamped R, B and G signals are respectively fed to pin 12, pin 5 and pin 2 of the analog switcher IC7 which are switched by the positive polarity vertical blanking pulse from pin 22 of CN4.

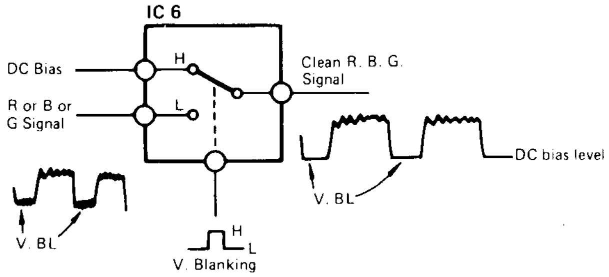


Fig. 7-2-3

The DC bias level is lower than the clamping level and the noise on the vertical blanking is eliminated by analog switcher IC7 which flows the DC bias during the vertical blanking.

The clean R, B and G signals are respectively fed to pin 10, pin 5 and pin 12 of the FET input operating amplifier IC8 which are functioned with diodes (D3, D4, D5) as peak detector/hold circuit.

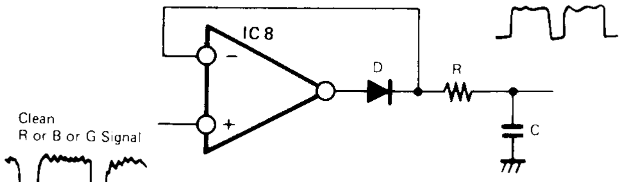


Fig. 7-2-4

The peak detected signal is fed to the integrator (R23/C19 for R signal, R24/C20 for B signal and R25/C21 for G signal) for the quasi DC level.

The analog switcher IC9 is functioned for resetting the discharge of capacitors C19, C20 C21 to be integrator and is controlled by the reset pulse from pin 7 of the microprocessor IC14 through the inverter Q9.

The microprocessor IC14 has the low (0V) or high (5V) level output.

The analog switcher IC9 is used in 9V circuit so that the control pulse should be 9V/0V. The inverter Q9 changes the polarity and level (from 5V/0V to 9V/0V) of the reset pulse for IC9.

When the reset pulse is fed at pin 9, 10, 11 of IC9, the analog switch IC9 is set to L position so that the capacitors C19, C20, C21 are discharged and the integrators (R23/C19, R24/C20, R25/C21) are functioned when the analog switch IC9 is set to H position by the high level at pin 9, 10, 11 of IC9.

The quasi DC level of R signal is fed to pin 13 of IC3(c) and the quasi DC level of B signal is fed to pin 12 of IC3(c). The quasi DC level of G signal is fed to pin 6 of the comparator IC8(b).

The analog switcher IC3(c) is controlled by the B/R selection pulse at pin 11 of IC3 from pin 20 of IC15 through the inverter Q10.

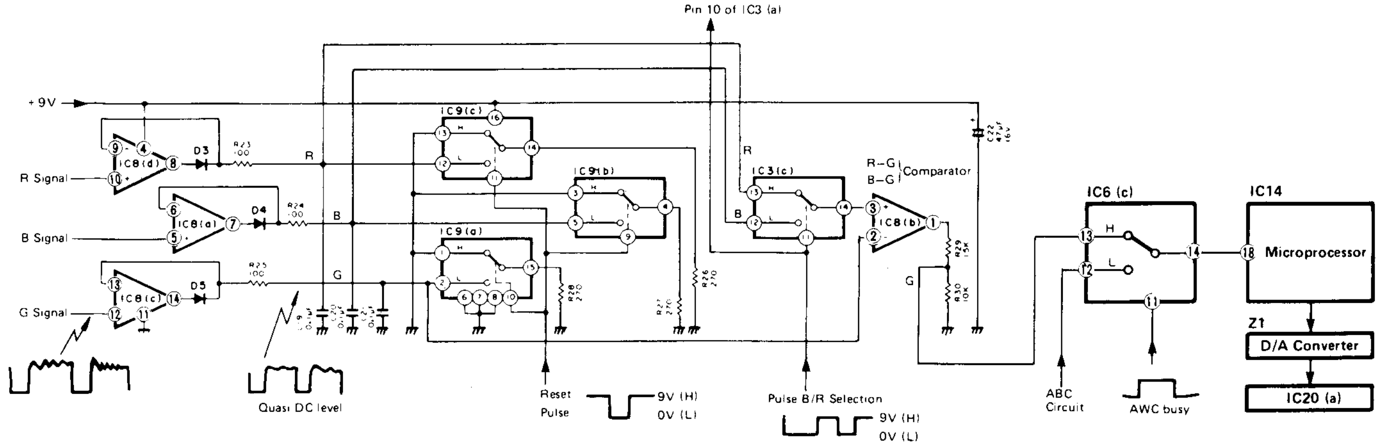

Pin 10 of IC3 (a)
+9V
R Signal
B Signal
G Signal
IC8(d)
IC8(a)
IC8(c)
D3
D4
D5
R23 100
R24 100
R25 100
R
B
G
C19 0.1μF
C20 0.1μF
C21 0.1μF
IC9(c)
IC9(b)
IC9(a)
H
L
R26 270
R27 270
R28 270
Quasi DC level
Reset Pulse
9V (H)
0V (L)
IC3(c)
R-G
B-G
Comparator
IC8(b)
C22 47μF 16V
R29 15K
R30 10K
Pulse B/R Selection
9V (H)
0V (L)
IC6 (c)
ABC Circuit
AWC busy
IC14
Microprocessor
Z1
D/A Converter
IC20 (a)

Fig. 7-2-5

The low (L) level of the control pulse is fed at first so that the quasi DC level of B signal at pin 12 of IC3(c) is fed to pin 3 of the comparator IC8(b). The high (H) or low (L) output at pin 1 of IC8(b) is fed to pin 13 of the analog switcher IC6(c) which is controlled by the AWC busy pulse at pin 11 of IC6(c) from pin 11 of IC14.

When the AWC busy pulse is fed to pin 11 of IC6(c), the analog switch is set to H position so that the output of the comparator IC8(b) is fed to pin 18 of IC14 through pin 14 of IC6(c).

If the B signal is higher than G signal, the output of IC8(b) is high (H) and the microprocessor IC14 instructs the count down digital code to D/A converter Z1 for reducing the blue(B) gain in Process board through the buffer IC20(a), the analog switcher IC19 and IC21. If the B signal is lower than G signal, the output of IC8(b) is low (L) and the microprocessor IC14 instructs the countup digital code to D/A converter Z1 for increasing the blue (B) gain in Process board. The red (R) gain in Process board is also controlled as similar way. The adjustment for blue (B) and red (R) are alternately carried.

The microprocessor IC14 sends 8-bit digital code to D/A converter for converting to analog DC level which is fed from pin 10 of Z1 to pin 3 of the buffer IC20(a). The analog DC level at pin 1 of IC20(a) is fed to pin 3 of the analog switcher IC18 and IC19 which switch is positioned by the pulse signals at pin 9/10/11 of IC18 and IC19.

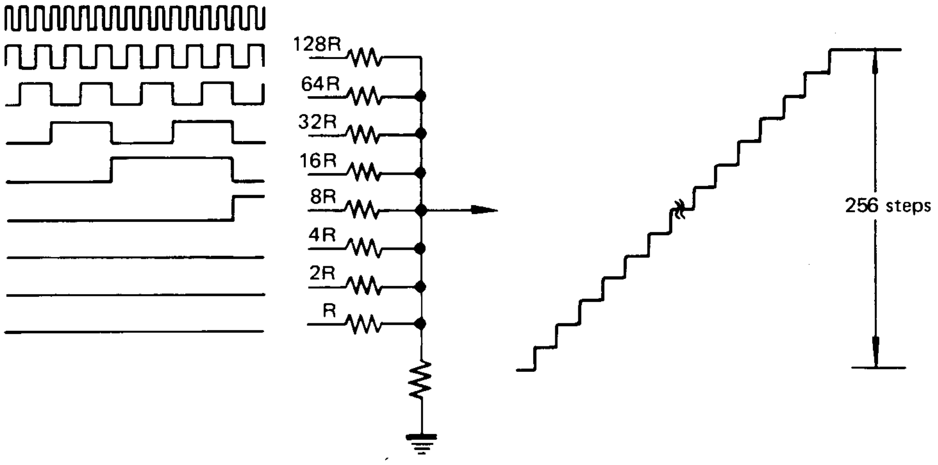

128R
64R
32R
16R
8R
4R
2R
R
256 steps

Fig. 7-2-6 D/A Converter Z1

The pulse signals at pin 9/10/11 of IC18 and IC19 are provided from the pin 4/3/2 of the microprocessor IC14 respectively.

The flow of the analog DC level in the IC18 and IC19 is controlled by the inhibit signal at pin 6 of IC18 and IC19. The inhibit signal for IC18 is provided from pin 5 of IC14 and the inhibit signal for IC19 is provided from pin 6 of IC14.

The analog DC level for the B signal is fed to pin 3 of IC22(a) from pin 5 of the analog switcher IC19 and is fed to the Process board through the mother board. The analog DC level for the R signal is fed to pin 5 of IC20(b) from pin 5 of the analog switcher IC18 and is fed to the Process board through the mother board. These procedure is continued until the color different signal B-G and R-G at IC8(b) becomes minimum. As a result, the B and R signal level match the G signal level automatically and the white balance setting is accomplished.

7-3 Auto Centering Control (ACC) Circuit

Outline

This circuit is automatically made the horizontal(H) and vertical(V) centering adjustment of red(R) and blue(B) image for matching them with the green(G) image by minimizing the color different signals (G-R) and (G-B). The color different signals (G-R) and (G-B) are minimized by utilizing the microprocessor which instructs the change of the DC voltage to the deflection coils for the R and B pick-up tube.

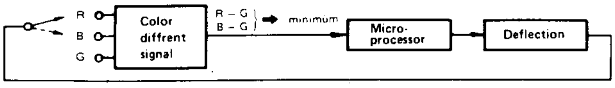


Fig. 7-3-1

Details

When the auto/manual centering selection switch on the side of the camera is set to the Auto position and the auto centering set switch on the front of the camera is set to the SET position, the low (L) ACC start pulse is fed to the pin 15 of IC15 through the input interface IC16(c), pin 6 of CN4 on this board (also pin 6 of CN4 on the mother board), C6 and pin 1 of BI2 on the mother board, pin 1 of CN40 and pin 6 of CN41 on the centering control board as starting of the auto centering circuit.

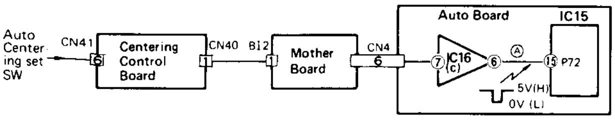


Fig. 7-3-2

The chroma signals R, B and G from the Process-2 board are respectively fed to the buffer Q1, Q2 and Q3 through pin 3, 5, 7 of CN4. These buffers are used for converting the high impedance to low impedance by emitter follow and also separated from the Process-2 board electronically.

The R signal is fed from the emitter of buffer Q1 to pin 1 of IC3(a), the B signal is fed from the emitter of buffer Q2 to pin 2 of IC3(a) and the G signal is fed from the emitter of buffer Q3 to pin 1 of comparator IC1.

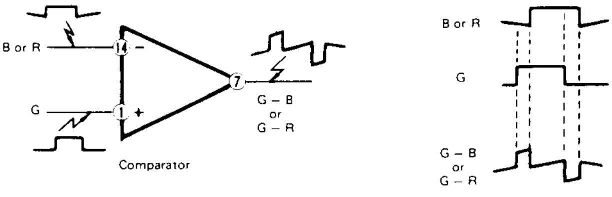
The R/B selector IC3(a) is controlled by IC15 which provides the high/low level (9V/0V) at the pin 10 of IC3(a) through the inverter Q10 from the pin 20 of IC15. The IC15 has the low (0V) or high (5V) level output so that the inverter Q10 changes the high level from 5V to 9V to switch the input of the IC3(a) which is 9V circuit.

The R signal at the pin 1 of IC3(a) and B signal at the pin 2 of IC3(a) is switched by the pulse signal at the pin 10 of IC3(a) according to the high/low level, and the output at the pin 15 of IC3(a) becomes as follows;

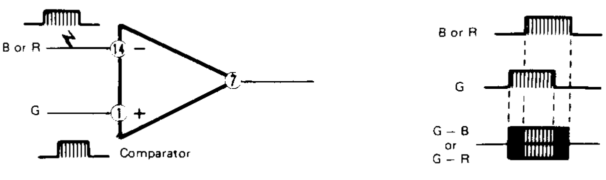
Pin 10	Pin 15
Low	B signal
High	R signal

The R or B signal selected by IC3(a) is fed to pin 14 of comparator IC1.

The color different signal (G-R) or (G-B) is made by the comparator IC1 which has the red(R) or blue(B) signal at the pin 14 of IC1 and the green(G) signal at pin 1 of IC1.



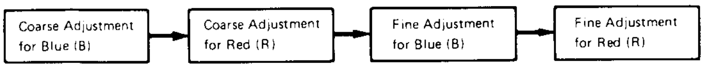
H Rate Waveform



V Rate Waveform

Fig. 7-3-3

The IC15 is programmed to start the high level pulse signal at pin 20 of IC15 which is inverted by Q10 to low level and fed to the pin 10 of IC3(a) so that the color different signal (G-B) is selected to be output at first, then (G-R) signal is selected as coarse centering adjustment as a cycle. After coarse centering adjustment, the fine centering adjustment for (G-B) and (G-R) signals is carried for the auto centering as;


Coarse Adjustment for Blue (B)
Coarse Adjustment for Red (R)
Fine Adjustment for Blue (B)
Fine Adjustment for Red (R)

These sequence are controlled by the analog switcher IC3(a) which is controlled by the pulse signal from pin 20 of IC15.

The color differential signal (G-R) and (G-B) at the output of the comparator IC1 is shown at the whole period of the signal which including blanking period. To be accurate auto centering, the center area of the images requires the most severe registration so that the window area at the center of the images is selected for the auto centering. Therefore, the color different signal (G-B)/(G-R) at pin 5 of IC3(b) should be controlled by the composite gate pulse at pin 9 of IC3(b) which is for window area, and the gated (G-B)/(G-R) signal at pin 4 of IC3(b) is fed to differentiator C26 and R33.

The gate pulse is generated by using monostable multivibrators IC4 and IC5.

The negative horizontal scanning start (Hs) pulse is fed from pin 20 of CN4 to pin 12 of IC4(b) which is triggered by rising part of Hs. The output at pin 9 of IC4(b) is the negative pulse with variable width changed by VR1. The back edge of the negative pulse at pin 9 of IC4(b) is adjusted by VR1 to 25 μsec from the front edge of Hs and fed to pin 4 of IC4(a). The monostable multivibrator IC4(a) is triggered by rising part of the negative pulse at pin 4 of IC4(a) and the output of the negative pulse at pin 7 of IC4(a) is obtained. The width of the negative pulse at pin 7 of IC4(a) is adjusted by VR2 to 25 μsec for horizontal gate for the window. The negative vertical blanking pulse is fed from pin 22 of CN4 to pin 12 of IC5(b) which is triggered by rising part of V blanking pulse.

The output at pin 9 of IC5(b) is the negative pulse with variable width changed by VR3. The width of the negative pulse at pin 9 of IC5 (b) is adjusted by VR3 to 7.2msec and fed to pin 4 of IC5 (a).

The monostable multivibrator IC5(a) is triggered by rising part of the negative pulse at pin 4 of IC5(a) and the output of the negative pulse at pin 7 of IC5(a) is obtained. The width of the negative pulse at pin 7 of IC5 (a) is adjusted by VR4 to 7.2 msec for vertical gate for the window.

The OR gate circuit consists of D1 and D2 and creates the composite gate signal for the window at the joint point of D1 and D2.

The composite gate signal is fed to pin 9 of IC3(b) for obtaining the gated (G-B)/(G-R) signal at pin 4 of IC3(b).

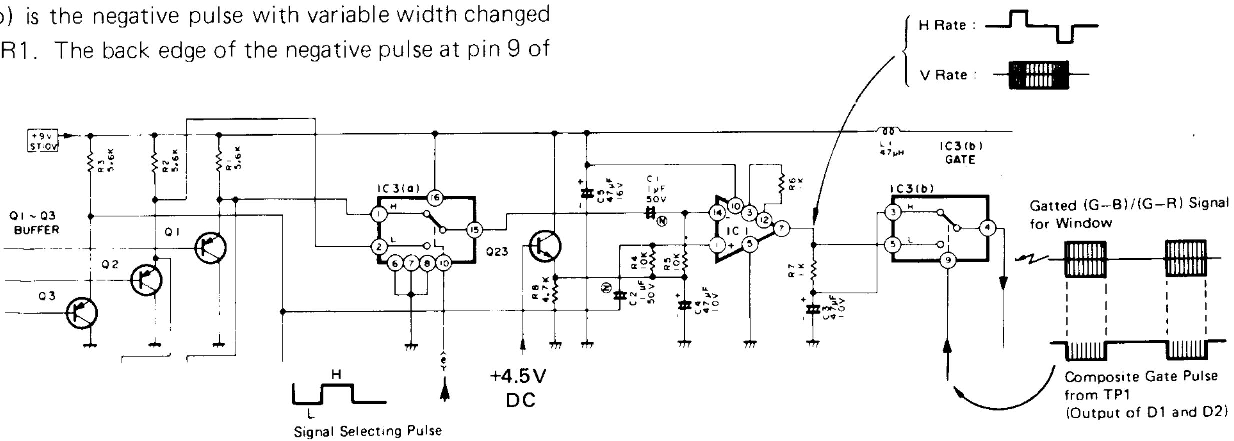

H Rate :
V Rate :
+9V ST:0V
R3 5.6K
R2 5.6K
R1 5.6K
Q1 ~ Q3 BUFFER
Q1
Q2
Q3
IC3(a)
H
L
16
1
2
15
6
7
8
10
Q23
R8 4.7K
C5 47μF 16V
C1 1μF 50V
N
C2 1μF 50V
R4 10K
R5 10K
C4 47μF 10V
IC1
14
10
3
12
7
1
5
R6 1K
R7 1K
C3 47μF 10V
L1 47μH
IC3(b) GATE
IC3(b)
3
5
4
9
Gatted (G−B)/(G−R) Signal for Window
Composite Gate Pulse from TP1 (Output of D1 and D2)
H
L
Signal Selecting Pulse from pin 20 of IC15 through Q10.
+4.5V DC

Fig. 7-3-4

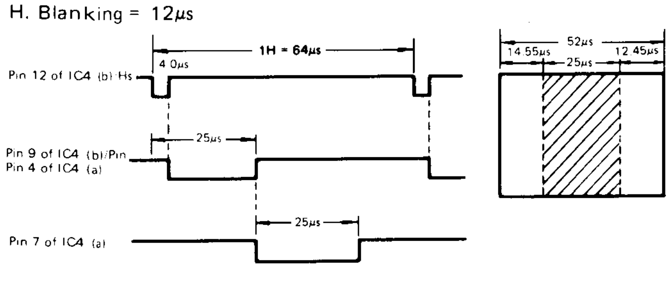

H. Blanking = 12μs
1H = 64μs
4.0μs
Pin 12 of IC4 (b) Hs
25μs
Pin 9 of IC4 (b)/Pin
Pin 4 of IC4 (a)
25μs
Pin 7 of IC4 (a)
52μs
14.55μs
12.45μs
25μs

Fig. 7-3-5

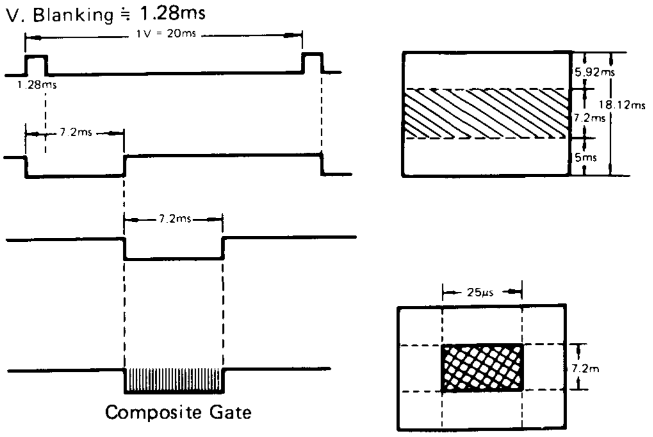

V. Blanking ≒ 1.28ms
1V = 20ms
1.28ms
7.2ms
7.2ms
Composite Gate
5.92ms
18.12ms
7.2ms
5ms
25μs
7.2m

Fig. 7-3-6

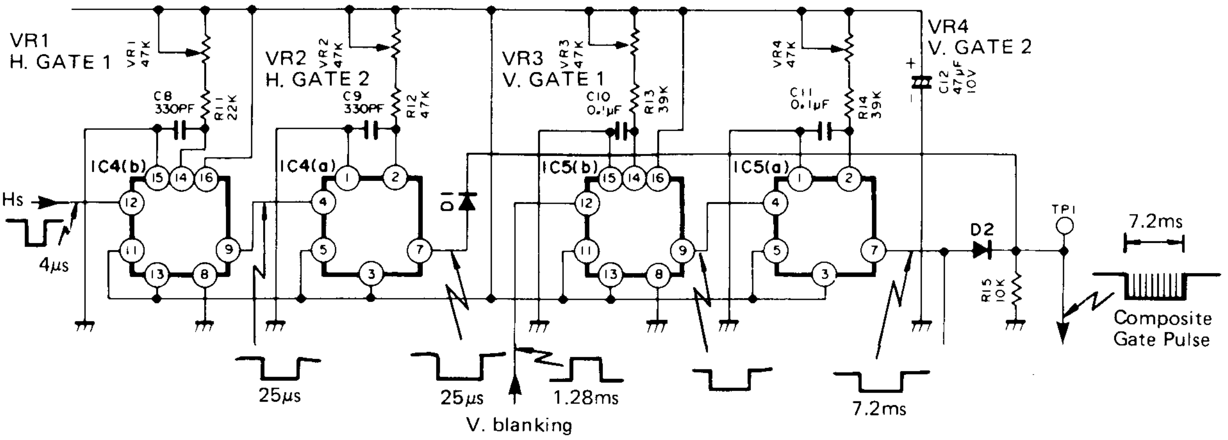

VR1
H. GATE 1
VR1 47K
C8 330PF
R11 22K
VR2
H. GATE 2
VR2 47K
C9 330PF
R12 47K
VR3
V. GATE 1
VR3 47K
C10 0.1μF
R13 39K
VR4 47K
C11 0.1μF
R14 39K
VR4
V. GATE 2
C12 47μF 10V
IC4(b)
IC4(a)
IC5(b)
IC5(a)
Hs
4μs
D1
D2
TP1
R15 10K
7.2ms
Composite Gate Pulse
25μs
25μs
1.28ms
V. blanking
7.2ms

Fig. 7-3-7

The gated (G-B)/(G-R) signal Ⓐ at pin 4 of IC3(b) is fed to the differentiator C26 and R33 as the high pass filter (H.P.F) for eliminating the low frequency portion in the gated (G-B)/(G-R) signal, and then detected by D6 to be only positive signal Ⓑ for the positive level microprocessors. The detected signal Ⓑ is fed to the integrator R34 and C27, and then fed to pin 5 of IC11(d) which is functioned with D7 and the integrator R37/C29 as peak hold circuit.

The detected/gated (G-B)/(G-R) signal from the pin 4 of IC3(b) is converted by peak hold circuit to the gated quasi DC signal Ⓔ which is proportional to the area of the detected/gated (R-B)/(R-G) signal, so that this gated quasi DC signal Ⓔ or Ⓕ becomes minimum when the auto centering is successfully completed. When the peak hold circuit is functioned, the C29 should be reset at first by Q13 which is controlled by the reset pulse at the base of Q13 from the pin 7 of the microprocessor IC14. The reset pulse is programmed in the microprocessors IC14 and IC15 to incorporate with the gated vertical pulse at the pin 7 of IC5(a). The gated vertical pulse is fed to the pin 3 of IC15. The IC11(a) is FET input operating amplifier and used as the buffer to prevent the leakage current from pin 4 of IC12(a) to C29.

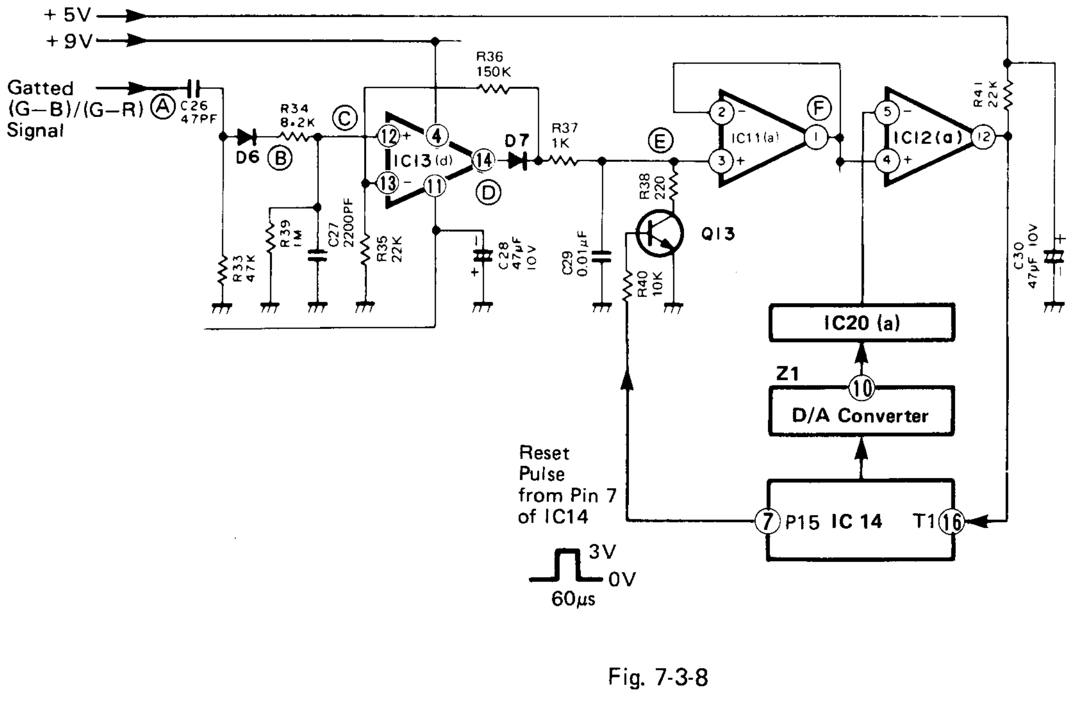

+5V
+9V
Gatted (G–B)/(G–R) Signal
Ⓐ
C26 47PF
R34 8.2K
Ⓒ
D6
Ⓑ
R33 47K
R39 1M
C27 2200PF
R35 22K
R36 150K
IC13(d)
D7
R37 1K
Ⓓ
C28 47μF 10V
C29 0.01μF
Ⓔ
R38 220
Q13
R40 10K
IC11(a)
Ⓕ
IC12(a)
R41 22K
C30 47μF 10V
IC20 (a)
Z1
D/A Converter
Reset Pulse from Pin 7 of IC14
P15 IC 14 T1
3V
0V
60μs

Fig. 7-3-8

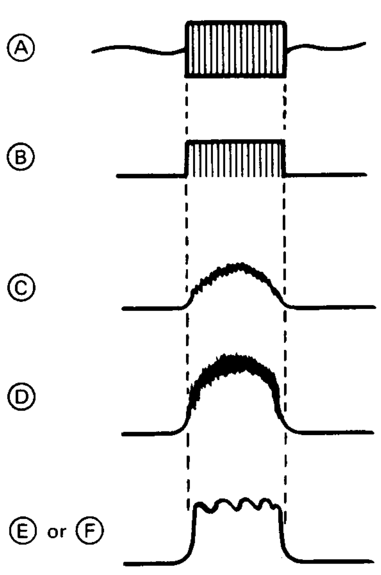


Fig. 7-3-9

The gated quasi DC signal Ⓕ is converted by programming in microprocessors IC14 and IC15 to the digital signal.

When the gated quasi DC signal Ⓕ is fed to pin 4 of comparator IC12(a) and the reset pulse from pin 7 of IC14 is fed to the base of Q13, the output at pin 12 of IC12(a) becomes high (H) level at first and is fed to pin 16 of IC14. The IC14 is programmed to make the output of the digital signal (8 bit coding) and converted to DC level by digital/analog (D/A) converter Z1.

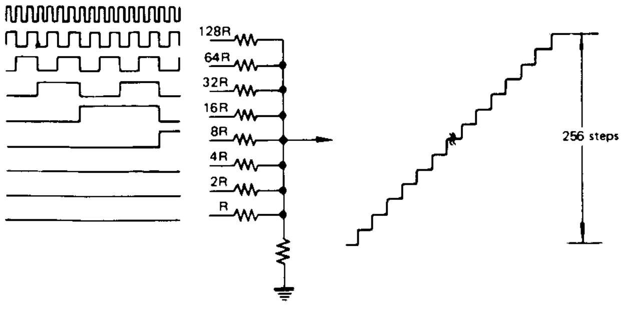
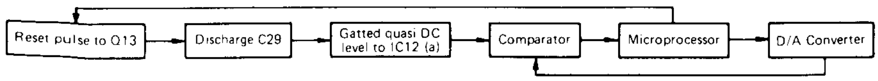


Fig. 7-3-10 D/A Converter Z1

The converted DC level by D/A Z1 is fed to pin 5 of IC12(a) through the buffer IC20(a) so that the quasi DC signal and the converted DC level can compared until the quasi DC level and the converted level are matched. Now the quasi DC signal level is identified by the microprocessor and memorized in form of digital signal. The conversion from DC level to digital signal (digital coding) is processed as;



To avoid the error function when the auto centering is setting against color object or scene, the digital signals are taken 30 times and then one average digital signal is programmed to be output.

It is better to select the fine object or scene for auto centering. The output of the average digital signal is converted by D/A converter Z1 to DC level which is output from pin 10 of Z1 to pin 3 of the buffer IC20(a). The DC level output at pin 1 of IC20(a) is fed to pin 3 of the switchers IC18 and IC19 which switch position is selected by the combination of the signal at 9, 10, 11 of IC18 and IC19 from IC14. The switcher IC18 and IC19 are handle 11 channel such as centering, blanking offset, gain control and pedestal control.

The DC level at pin 3 of IC18 and IC19 is controlled by the inhibit at pin 6 of IC18 and 19 which is controlled by IC14.

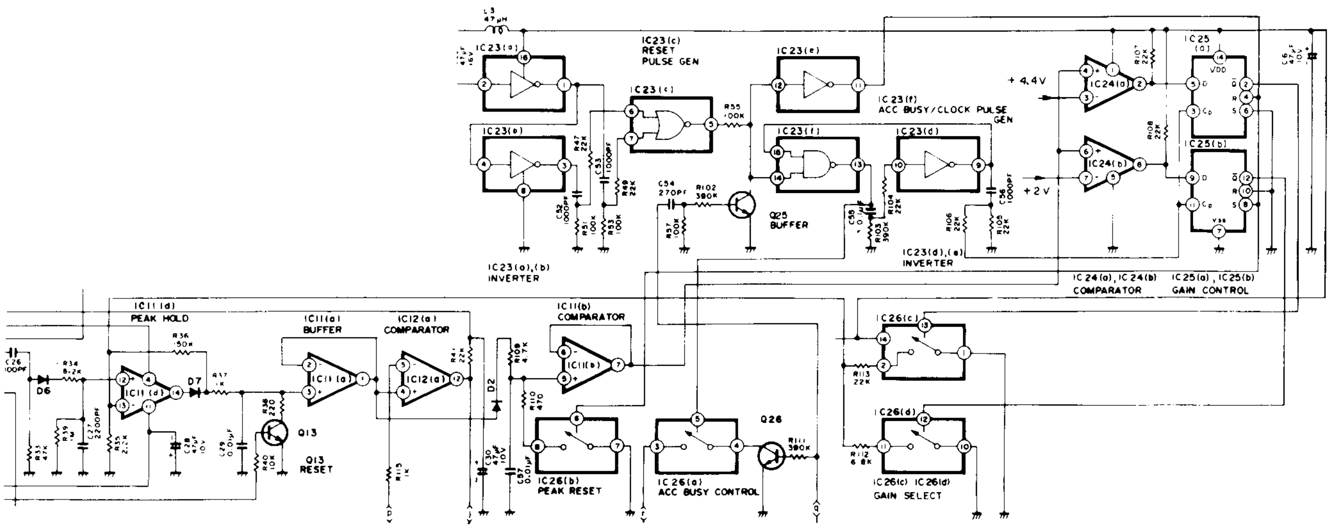
The DC level for the horizontal blue(B.H) is fed from pin 2 of IC18 to pin 12 of IC21(d) and the output at pin 14 of IC21(d) is fed to the deflection coil for the blue pick-up tube through the mother board, ACC-MANUAL select board and deflection board.

After this DC level is fed to the deflection coil, the new signal is generated. This new color different signal is again processed and compared with previous signal. If the new color different signal is larger than previous, the microprocessor IC14 instructs to output for reducing new color different signal. If the new color different signal is smaller than previous, the microprocessor IC14 instructs to output until the minimum color different signal is reached.

For accurate auto centering function, the gain of peak hold amplifier IC11(d) is changed to three state as;

	GAIN OF IC11(d)	IC26(c)	IC26(d)
(A)	+8 dB	ON	ON
(B)	0 dB	ON	OFF
(C)	-6 dB	OFF	OFF

The quasi DC signal level at pin 14 of IC11(d) is peak rectified by D2 and C57 and supplied to the window comparator IC24(a) and IC24(b) through buffer IC11(b). The window voltage is set from +2V (pin 7 of IC24(b)) to +4.4V (pin 3 of IC24(a)) and the output of IC24(a) and IC24(b) are fed to D-type flip-flop IC25(a) and IC25(b).


IC23(c) RESET PULSE GEN
IC23(a)
IC23(b)
IC23(c)
IC23(e)
IC23(f)
IC23(d)
IC 23(f) ACC BUSY/CLOCK PULSE GEN
IC23(a),(b) INVERTER
IC23(d),(e) INVERTER
Q25 BUFFER
+4.4V
+2V
IC24(a)
IC24(b)
IC25 (a)
IC25(b)
IC24(a), IC24(b) COMPARATOR
IC25(a), IC25(b) GAIN CONTROL
IC11(d) PEAK HOLD
IC11(a) BUFFER
IC12(a) COMPARATOR
IC11(b) COMPARATOR
Q13 RESET
IC26(b) PEAK RESET
IC26(a) ACC BUSY CONTROL
Q26
IC26(c)
IC26(d)
IC26(c) IC26(d) GAIN SELECT
D6
D7
D2

As a result, the output of IC25(a) and IC25(b) are changed as follows.

Quasi DC level	0V - 2V	2V - 4.4V	4.4V - 9V
pin 2 of IC24(a)	L	L	H
pin 8 of IC24(a)	L	H	H
pin 2 of IC25(a)	H	H	L
pin 12 of IC25(b)	H	L	L
Registration error	SMALLER	SMALL	LARGE

In this way, the gain of IC11(d) is controlled for accurate auto centering function.

IC23(a), IC23(b), IC23(c) and IC23(e) are reset pulse generator for IC25(a) and IC25(b). The R/B select pulse from pin 20 of IC15 through inverter Q10 is fed to pin 2 of IC23(a) and the reset pulse is generated at the beginning of R or B selecting pulse and is fed to pin 4 of IC25(a) and pin 8 of IC25(b) to reset the output of IC25 as (B) state (0 dB).

A monostable multivibrator consisting of IC23(f) and IC23(d) generates 20 msec clock pulse from the reset pulse supplied at pin 14 of IC23(f), and is supplied to pins 3 and 11 of IC25. This clock pulse is also supplied to pin 5 of IC26(a) in order to pause the microprocessor IC14 during 20 msec. The ACC BUSY pulse is supplied from pin 14 of IC14 to the base of Q26 in order to function IC26(a) only for automatic centering function. This ACC BUSY pulse is also fed to the base of Q25 through differentiator C54 and R57 as a start trigger pulse for IC23(e), IC23(f) and IC23(d).

ORDER NO. VKD84060842S8

Service Manual

Vol. 3

Block Diagrams
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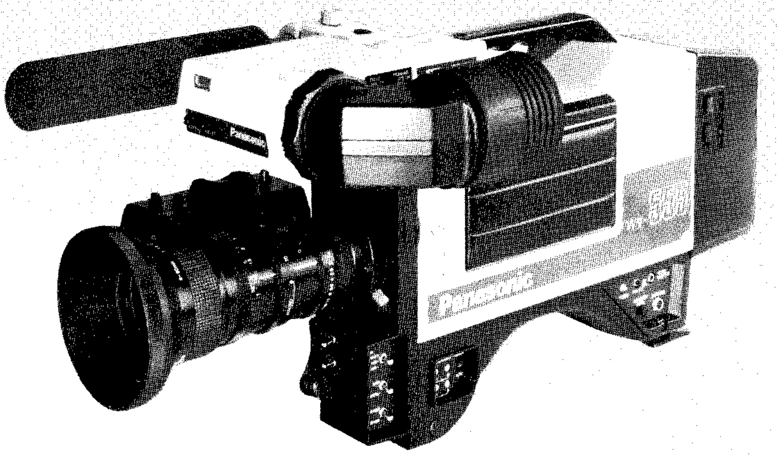

- The automatic centering control circuit on the Auto board has been changed to improve the function of automatic centering control from serial No. 41A00001 and higher.

- Please file this supplement service manual with the service manual order No. VKD83100784C8.

Panasonic

Matsushita Electric Trading Co., Ltd.
P.O. Box 288, Central Osaka Japan
Printed in Japan
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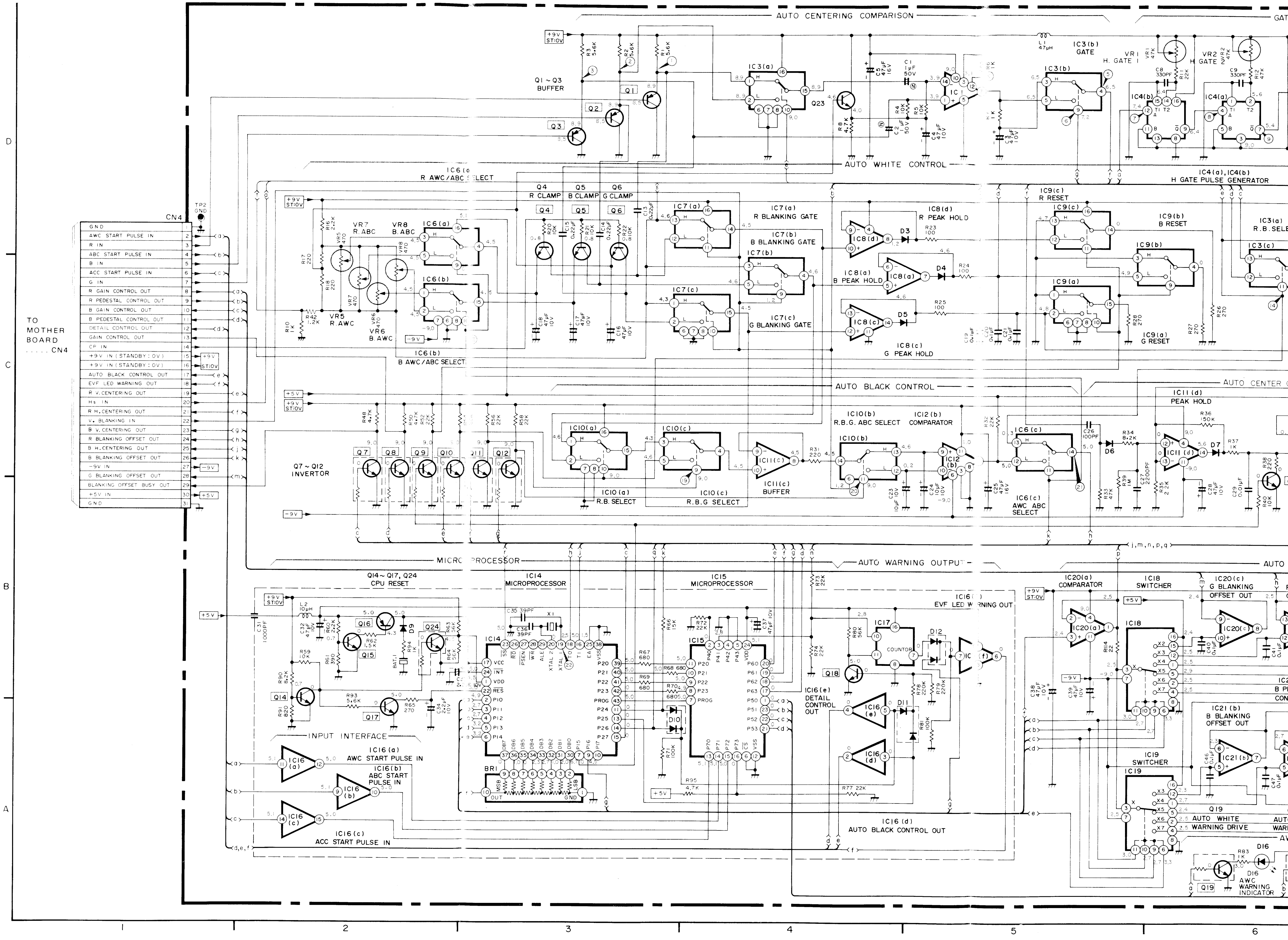
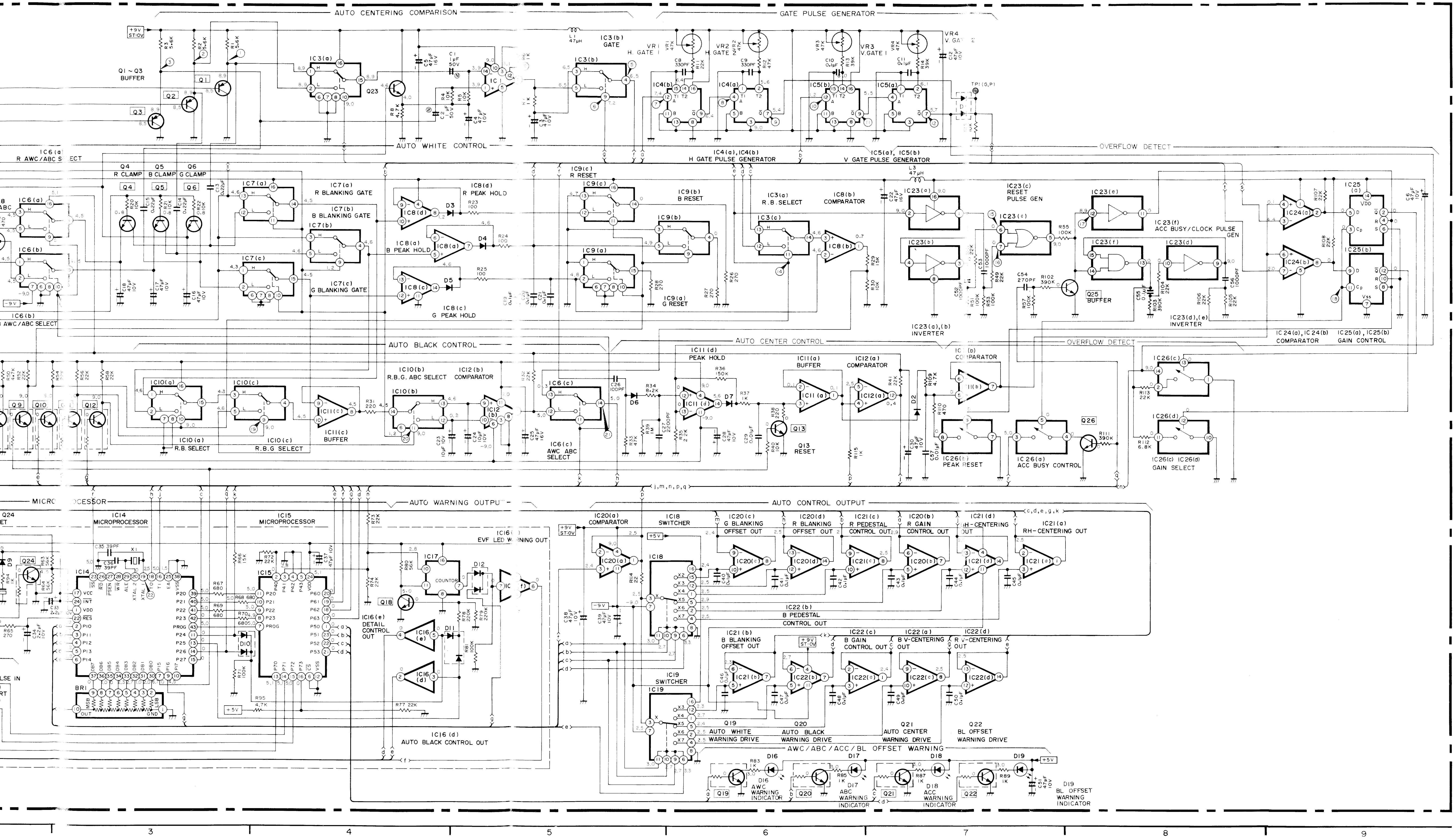
IC1	MC1733CP		D5
IC3	TC4053BF		C6, D4, D5
IC4	TC4538BF		D6
IC5	TC4538BF		D6, D7
IC6	TC4053BF		C2, D2, C5
IC7	TC4053BF		C4, D4
IC8	TL064CNS		C4. D4, C6
IC9	TC4053BF		C5, C6, D4
IC10	TC4053BF		C3, C4
IC11	TL064CNS		C6, C7, C4
IC12	UPC272G		C5, C6, C7
IC14	80C4952GSK		A3, B3
IC15	82C43GSK		A4, B4
IC16	TC4050BF		A2, A4, A5
IC17	TC4020BF		A4
IC18	TC4051BF		A5, A6, B5, B6
IC19	TC4051BF		A5, A6
IC20	TL064CNS		B5, B6, B7
IC21	TL064CNS		A6, B6, B7
IC22	TL064CNS		A6, A7
IC23	HD14572UBP		C7, C8
IC24	AN6913		C9
IC25	TC4013BF		C9
IC26	TC4066BF		C7, C8
Q1	2SB709-QRS	(A)	D3
Q2	2SB709-QRS	(A)	D3
Q3	2SB709-QRS	(A)	D3
Q4	2SD601-QRS	(Y)	C3
Q5	2SD601-QRS	(Y)	C3
Q6	2SD601-QRS	(Y)	C3
Q7	UN2217TW		C2
Q8	UN2217TW		C2
Q9	UN2217TW		C2
Q10	UN2217TW		C2
Q11	UN2217TW		C3
Q12	UN2217TW		C3
Q13	2SD602-QR	(W)	B6
Q14	2SD601-QRS	(Y)	B2
Q15	2SD601-QRS	(Y)	B2
Q16	2SB793-QR		B2
Q17	2SB793-QR		A2
Q18	2SD601-QRS	(Y)	A4
Q19	UN2217TW		A6
Q20	UN2217TW		A6
Q21	UN2217TW		A7
Q22	UN2217TW		A7
Q23	2SD601-QRS	(Y)	D4
Q24	UN2217TW		B2
Q25	2SD601-QRS	(Y)	C7
Q26	2SD601-QRS	(Y)	B8
D1	MA151K	(MH)	D7
D2	MA151K	(MH)	C7
D3	MA151K	(MH)	C4
D4	MA151K	(MH)	C5
D5	MA151K	(MH)	C4
D6	1SS99		C5
D7	MA151K	(MH)	C6
D9	MA151K	(MH)	B2
D10	MA151K	(MH)	A3
D11	MA151K	(MH)	A4
D12	MA151K	(MH)	A5
D16	SEL1121R		A6
D17	SEL1121R		A6
D18	SEL1121R		A7
D19	SEL1121R		A7

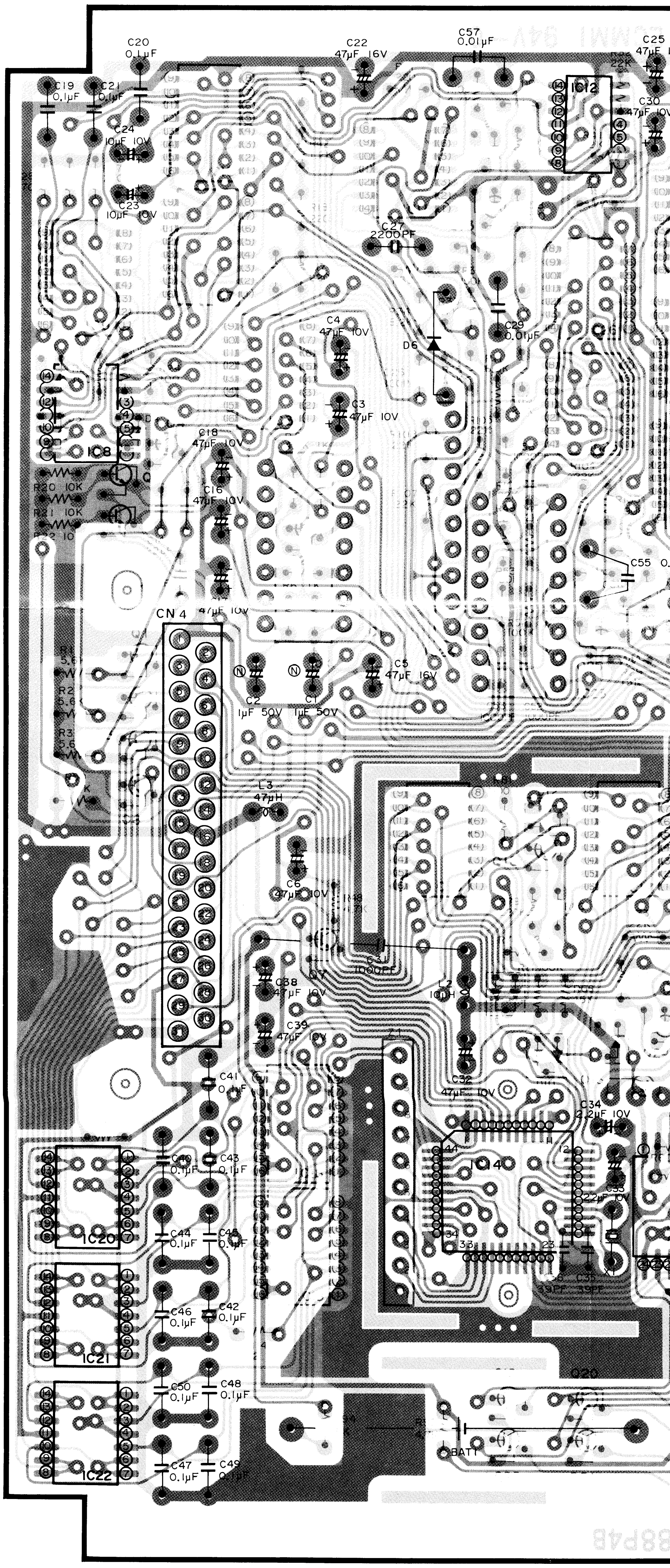
SCHEMATIC DIAGRAM OF AUTO BOARD


D
C
B
A
1
2
3
4
5
6
TO MOTHER BOARD CN4
CN4
TP2 GND
GND
AWC START PULSE IN
R IN
ABC START PULSE IN
B IN
ACC START PULSE IN
G IN
R GAIN CONTROL OUT
R PEDESTAL CONTROL OUT
B GAIN CONTROL OUT
B PEDESTAL CONTROL OUT
DETAIL CONTROL OUT
GAIN CONTROL OUT
CP IN
+9V IN (STANDBY:0V)
+9V IN (STANDBY:0V)
AUTO BLACK CONTROL OUT
EVF LED WARNING OUT
R V.CENTERING OUT
Hs IN
R H.CENTERING OUT
V. BLANKING IN
B V.CENTERING OUT
R BLANKING OFFSET OUT
B H.CENTERING OUT
B BLANKING OFFSET OUT
-9V IN
G BLANKING OFFSET OUT
BLANKING OFFSET BUSY OUT
+5V IN
GND
AUTO CENTERING COMPARISON
Q1 ~ Q3 BUFFER
IC3(a)
Q23
IC1
IC3(b) GATE
H. GATE I
H GATE 2
IC4(a), IC4(b) H GATE PULSE GENERATOR
AUTO WHITE CONTROL
IC6(a) R AWC/ABC SELECT
VR7 R ABC
VR8 B.ABC
VR5 R AWC
VR6 B AWC
IC6(b) B AWC/ABC SELECT
Q4 R CLAMP
Q5 B CLAMP
Q6 G CLAMP
IC7(a) R BLANKING GATE
IC7(b) B BLANKING GATE
IC7(c) G BLANKING GATE
IC8(d) R PEAK HOLD
IC8(a) B PEAK HOLD
IC8(c) G PEAK HOLD
IC9(c) R RESET
IC9(b) B RESET
IC9(a) G RESET
IC3(a) R.B.SELECT
AUTO BLACK CONTROL
IC10(b) R.B.G. ABC SELECT
IC12(b) COMPARATOR
IC10(a) R.B. SELECT
IC10(c) R.B.G SELECT
IC11(c) BUFFER
Q7 ~ Q12 INVERTOR
IC6(c) AWC ABC SELECT
IC11(d) PEAK HOLD
AUTO CENTER
MICROPROCESSOR
AUTO WARNING OUTPUT
AUTO
Q14 ~ Q17, Q24 CPU RESET
IC14 MICROPROCESSOR
IC15 MICROPROCESSOR
IC16(f) EVF LED WARNING OUT
IC17 COUNTOR
IC16(e) DETAIL CONTROL OUT
IC16(d) AUTO BLACK CONTROL OUT
INPUT INTERFACE
IC16(a) AWC START PULSE IN
IC16(b) ABC START PULSE IN
IC16(c) ACC START PULSE IN
BR1
IC20(a) COMPARATOR
IC18 SWITCHER
IC20(c) G BLANKING OFFSET OUT
IC21(b) B BLANKING OFFSET OUT
IC19 SWITCHER
Q19 AUTO WHITE WARNING DRIVE
D16 AWC WARNING INDICATOR

SCHEMATIC DIAGRAM OF AUTO BOARD


AUTO CENTERING COMPARISON
GATE PULSE GENERATOR
Q1 ~ Q3 BUFFER
IC3(a)
IC3(b) GATE
VR1 H. GATE I
VR2 H GATE 2
VR3 V.GATE I
VR4 V. GATE 2
IC4(a), IC4(b) H GATE PULSE GENERATOR
IC5(a), IC5(b) V GATE PULSE GENERATOR
AUTO WHITE CONTROL
OVERFLOW DETECT
IC6(a) R AWC/ABC SELECT
IC6(b) B AWC/ABC SELECT
Q4 R CLAMP
Q5 B CLAMP
Q6 G CLAMP
IC7(a) R BLANKING GATE
IC7(b) B BLANKING GATE
IC7(c) G BLANKING GATE
IC8(d) R PEAK HOLD
IC8(a) B PEAK HOLD
IC8(c) G PEAK HOLD
IC9(c) R RESET
IC9(b) B RESET
IC9(a) G RESET
IC3(a) R.B. SELECT
IC8(b) COMPARATOR
IC23(a), (b) INVERTER
IC23(c) RESET PULSE GEN
IC23(f) ACC BUSY/CLOCK PULSE GEN
Q25 BUFFER
IC23(d), (e) INVERTER
IC24(a), IC24(b) COMPARATOR
IC25(a), IC25(b) GAIN CONTROL
AUTO BLACK CONTROL
AUTO CENTER CONTROL
IC10(a) R.B. SELECT
IC10(c) R.B.G SELECT
IC11(c) BUFFER
IC10(b) R.B.G. ABC SELECT
IC12(b) COMPARATOR
IC6(c) AWC ABC SELECT
IC11(d) PEAK HOLD
IC11(a) BUFFER
IC12(a) COMPARATOR
Q13 RESET
IC11(b) COMPARATOR
IC26(f) PEAK RESET
IC26(a) ACC BUSY CONTROL
Q26
IC26(c) IC26(d) GAIN SELECT
MICROPROCESSOR
IC14 MICROPROCESSOR
IC15 MICROPROCESSOR
BR1
AUTO WARNING OUTPUT
IC16(f) EVF LED WARNING OUT
IC17 COUNTOR
Q18
IC16(e) DETAIL CONTROL OUT
IC16(d) AUTO BLACK CONTROL OUT
AUTO CONTROL OUTPUT
IC20(a) COMPARATOR
IC18 SWITCHER
IC20(c) G BLANKING OFFSET OUT
IC20(d) R BLANKING OFFSET OUT
IC21(c) R PEDESTAL CONTROL OUT
IC20(b) R GAIN CONTROL OUT
IC21(d) RH-CENTERING OUT
IC21(a) RH-CENTERING OUT
IC22(b) B PEDESTAL CONTROL OUT
IC21(b) B BLANKING OFFSET OUT
IC22(c) B GAIN CONTROL OUT
IC22(a) B V-CENTERING OUT
IC22(d) R V-CENTERING OUT
IC19 SWITCHER
Q19 AUTO WHITE WARNING DRIVE
Q20 AUTO BLACK WARNING DRIVE
Q21 AUTO CENTER WARNING DRIVE
Q22 BL OFFSET WARNING DRIVE
AWC/ABC/ACC/BL OFFSET WARNING
D16 AWC WARNING INDICATOR
D17 ABC WARNING INDICATOR
D18 ACC WARNING INDICATOR
D19 BL OFFSET WARNING INDICATOR
+9V ST:0V
+5V
-9V
3
4
5
6
7
8
9

CONDUCTOR VIEW OF AUTO BOARD



D
C
B
A
1
2
3
C20 0.1μF
C22 47μF 16V
C57 0.01μF
C25 47μF
C19 0.1μF
C21 0.1μF
IC12
C30 47μF
C24 10μF 10V
C23 10μF 10V
C27 2200PF
C4 47μF 10V
C29 0.01μF
D6
C3 47μF 10V
C18 47μF 10V
IC8
R20 10K
R21 10K
C16 47μF 10V
C55
CN4
C5 47μF 16V
C2 1μF 50V
C1 1μF 50V
L3 47μH
C6 47μF 10V
C38 47μF 10V
C39 47μF 10V
C31
L2
C32 47μF 10V
C34 2.2μF 10V
C41 0.1μF
C40 0.1μF
C43 0.1μF
IC14
IC20
C44 0.1μF
C45
C46 0.1μF
C42 0.1μF
IC21
C50 0.1μF
C48 0.1μF
Q20
BATT
C47 0.1μF
C49
IC22

TO
MOTHER
BOARD
..... CN4

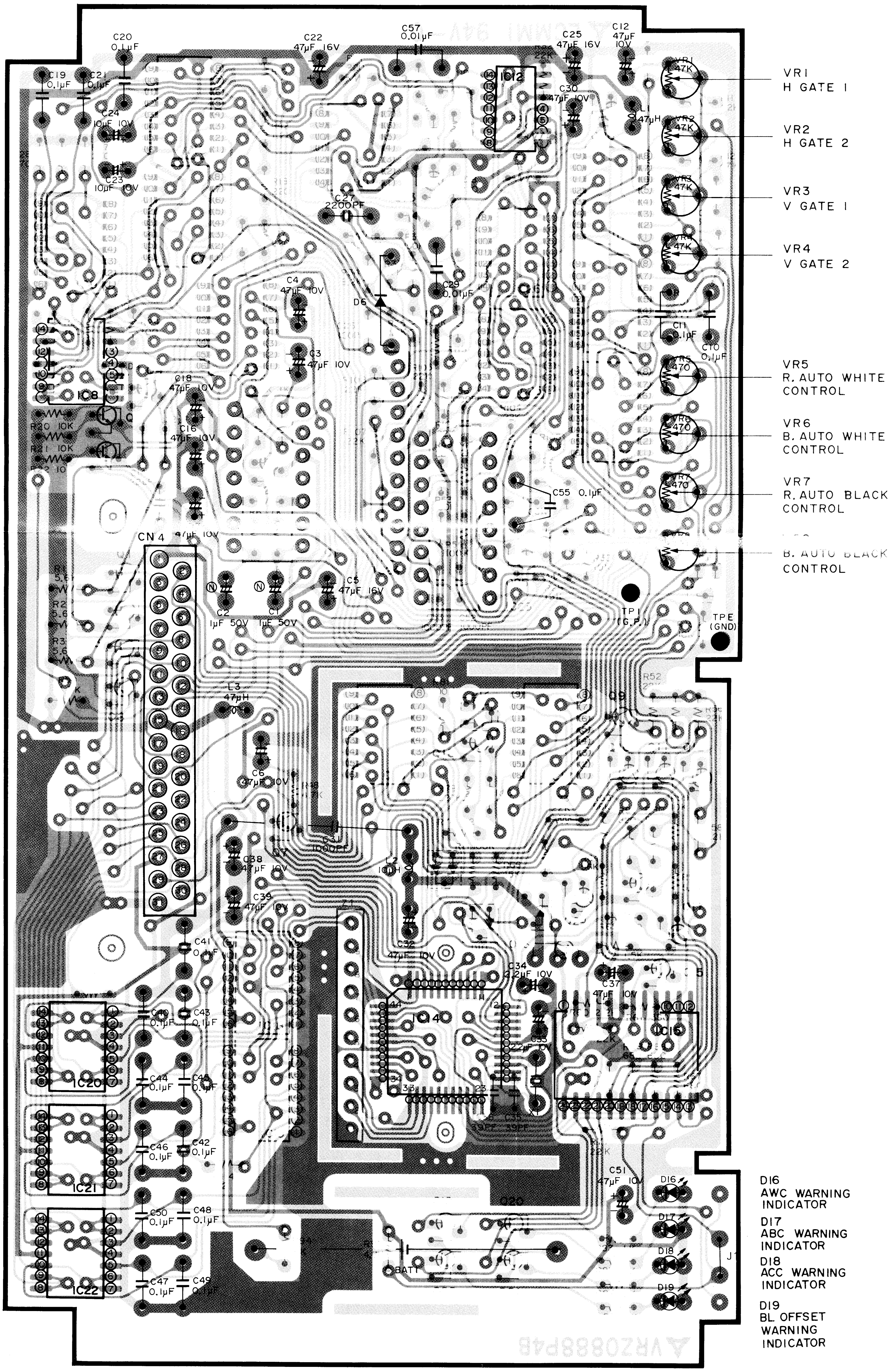
	CN4
GND	1
AWC START PULSE IN	2
R IN	3
ABC START PULSE IN	4
B IN	5
ACC START PULSE IN	6
G IN	7
R GAIN CONTROL OUT	8
R PEDESTAL CONTROL OUT	9
B GAIN CONTROL OUT	10
B PEDESTAL CONTROL OUT	11
DETAIL CONTROL OUT	12
GAIN CONTROL OUT	13
CP IN	14
+9V IN (STANDBY : 0V)	15
+9V IN (STANDBY : 0V)	16
AUTO BLACK CONTROL OUT	17
EVF LED WARNING OUT	18
R V-CENTERING OUT	19
Hs IN	20
R H-CENTERING OUT	21
V. BLANKING IN	22
B V-CENTERING OUT	23
R BLANKING OFFSET OUT	24
B H-CENTERING OUT	25
B BLANKING OFFSET OUT	26
-9V IN	27
G BLANKING OFFSET OUT	28
BLANKING OFFSET BUSY OUT	29
+5V IN	30
GND	31

IC1	MC1733CP	C2	IC15	82C43GSK	A3	Q1	2SB709-QRS	(A)	C2	Q14	2SD601-QRS
IC3	TC4053BF	C2	IC16	TC4050BF	B2, C3	Q2	2SB709-QRS	(A)	B2	Q15	2SD601-QRS
IC4	TC4538BF	C3, D3	IC17	TC4020BF	B3	Q3	2SB709-QRS	(A)	B2	Q16	2SB793-QR
IC5	TC4538BF	C3	IC18	TC4051BF	A2, B2	Q4	2SD601-QRS	(Y)	C2	Q17	2SD601-QRS
IC6	TC4053BF	C3	IC19	TC4051BF	A2	Q5	2SD601-QRS	(Y)	C2	Q18	2SD601-QRS
IC7	TC4053BF	C2, D2	IC20	TL064CNS	A2	Q6	2SD601-QRS	(Y)	C2	Q19	UN2217TW
IC8	TL064CNS	C2	IC21	TL064CNS	A2	Q7	UN2217TW		B2	Q20	UN2217TW
IC9	TC4053BF	C2, D2	IC22	TL064CNS	A2	Q8	UN2217TW		B2	Q21	UN2217TW
IC10	TC4053BF	D2	IC23	HD14572UBP	C3	Q9	UN2217TW		B3	Q22	UN2217TW
IC11	TL064CNS	D2	IC24	AN6913	C3	Q10	UN2217TW		B3	Q23	2SD601-QRS
IC12	UPC272G	D3	IC25	TC4013BF	C3	Q11	UN2217TW		B3	Q24	UN2217TW
IC14	80C4952GSK	A3	IC26	TC4066BF	C3	Q12	UN2217TW		B3	Q25	2SD601-QRS
						Q13	2SD602-QR	(W)	D3	Q26	2SD601-QRS

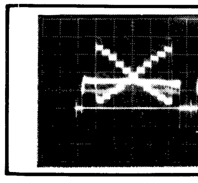
CONDUCTOR VIEW OF AUTO BOARD

SI

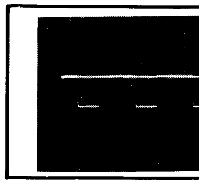
	CN4
	1
N	2
	3
N	4
	5
N	6
	7
	8
OUT	9
	10
OUT	11
	12
	13
	14
V)	15
V)	16
OUT	17
T	18
	19
	20
	21
	22
	23
UT	24
	25
UT	26
	27
UT	28
Y OUT	29
	30
	31


C20 0.1μF
C22 47μF 16V
C57 0.01μF
C25 47μF 16V
C12 47μF 10V
C19 0.1μF
C21 0.1μF
C24 10μF 10V
C23 10μF 10V
IC12
C30 47μF 10V
L1 47μH
C27 2200PF
C4 47μF 10V
C29 0.01μF
D6
C3 47μF 10V
C11 0.1μF
C10 0.1μF
IC8
R20 10K
R21 10K
C18 47μF 10V
C16 47μF 10V
C55 0.1μF
CN4
C5 47μF 16V
C2 1μF 50V
C1 1μF 50V
TP1 (G.P.)
TPE (GND)
L3 47μH
C6 47μF 10V
C38 47μF 10V
C39 47μF 10V
L2 10μH
C41 0.1μF
C32 47μF 10V
C34 2.2μF 10V
C37 47μF 10V
IC14
IC15
C40 0.1μF
C43 0.1μF
IC20
C44 0.1μF
C45 0.1μF
C46 0.1μF
C42 0.1μF
IC21
C50 0.1μF
C48 0.1μF
IC22
C47 0.1μF
C49 0.1μF
C51 47μF 10V
BATT
J1
VR20888P4B
VR1
H GATE 1
VR2
H GATE 2
VR3
V GATE 1
VR4
V GATE 2
VR5
R. AUTO WHITE CONTROL
VR6
B. AUTO WHITE CONTROL
VR7
R. AUTO BLACK CONTROL
B. AUTO BLACK CONTROL
D16
AWC WARNING INDICATOR
D17
ABC WARNING INDICATOR
D18
ACC WARNING INDICATOR
D19
BL OFFSET WARNING INDICATOR

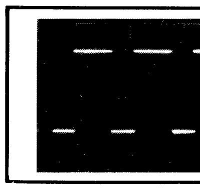
1 0.2V/DIV, 10μs/D



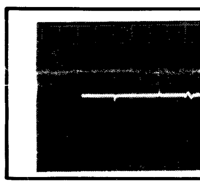
6 5V/DIV, 20μs/DI



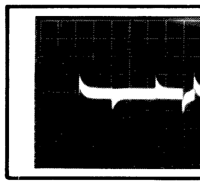
11 2V/DIV, 5ms/DI



16 20mV/DIV, 10μs



21 20mV/DIV, 10μs



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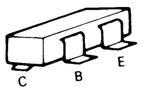
2SD602-QRS
UN2217TW



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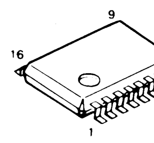
TC4053BF
TC4538BF



2

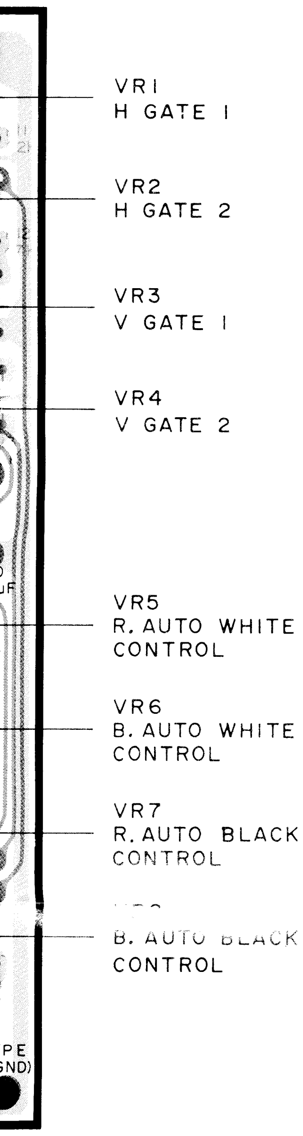
3

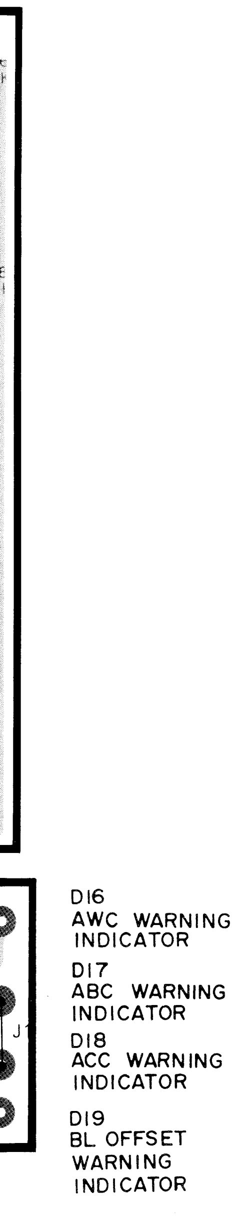
K	A3
F	B2, C3
F	B3
F	A2, B2
F	A2
S	A2
S	A2
S	A2
UBP	C3
	C3
F	C3
F	C3

Q1	2SB709-QRS	(A)	C2
Q2	2SB709-QRS	(A)	B2
Q3	2SB709-QRS	(A)	B2
Q4	2SD601-QRS	(Y)	C2
Q5	2SD601-QRS	(Y)	C2
Q6	2SD601-QRS	(Y)	C2
Q7	UN2217TW		B2
Q8	UN2217TW		B2
Q9	UN2217TW		B3
Q10	UN2217TW		B3
Q11	UN2217TW		B3
Q12	UN2217TW		B3
Q13	2SD602-QR	(W)	D3

Q14	2SD601-QRS	(Y)	D3
Q15	2SD601-QRS	(Y)	B3
Q16	2SB793-QR		B3
Q17	2SD601-QRS		B3
Q18	2SD601-QRS	(Y)	B2, B3
Q19	UN2217TW		A3
Q20	UN2217TW		A3
Q21	UN2217TW		A3
Q22	UN2217TW		A3
Q23	2SD601-QRS	(Y)	C2
Q24	UN2217TW		B3
Q25	2SD601-QRS	(Y)	C3
Q26	2SD601-QRS	(Y)	D3

D1	MA151K	(MH)	D3
D2	MA151K	(MH)	C3
D3	MA151K	(MH)	C2
D4	MA151K	(MH)	C2
D5	MA151K	(MH)	C2
D6	1SS99		C3
D7	MA151K	(MH)	C3, D3
D9	MA151K	(MH)	B3
D10	MA151K	(MH)	B3
D11	MA151K	(MH)	B3
D12	MA151K	(MH)	B3
D16	SEL1121R		A3
D17	SEL1121R		A3
D18	SEL1121R		A3
D19	SEL1121R		A3

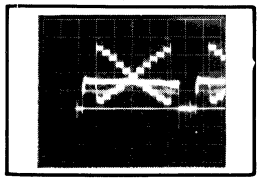

VR1
H GATE 1
VR2
H GATE 2
VR3
V GATE 1
VR4
V GATE 2
VR5
R. AUTO WHITE
CONTROL
VR6
B. AUTO WHITE
CONTROL
VR7
R. AUTO BLACK
CONTROL
B. AUTO BLACK
CONTROL


D16
AWC WARNING
INDICATOR
D17
ABC WARNING
INDICATOR
D18
ACC WARNING
INDICATOR
D19
BL OFFSET
WARNING
INDICATOR

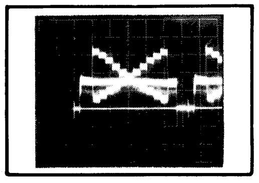
D1	MA151K	(MH)	D3
D2	MA151K	(MH)	C3
D3	MA151K	(MH)	C2
D4	MA151K	(MH)	C2
D5	MA151K	(MH)	C2
D6	1SS99		C3
D7	MA151K	(MH)	C3, D3
D9	MA151K	(MH)	B3
D10	MA151K	(MH)	B3
D11	MA151K	(MH)	B3
D12	MA151K	(MH)	B3
D16	SEL1121R		A3
D17	SEL1121R		A3
D18	SEL1121R		A3
D19	SEL1121R		A3

SIGNAL WAVEFORMS OF AUTO BOARD

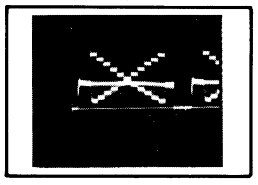
1 0.2V/DIV, 10μs/DIV



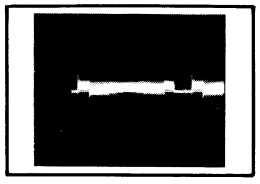
2 0.2V/DIV, 10μs/DIV



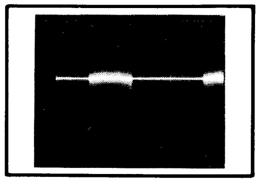
3 0.2V/DIV, 10μs/DIV



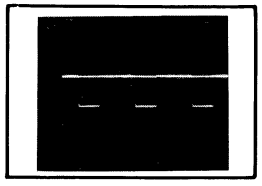
4 50mV/DIV, 10μs/DIV



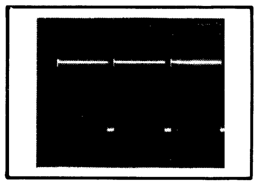
5 0.5V/DIV, 10μs/DIV



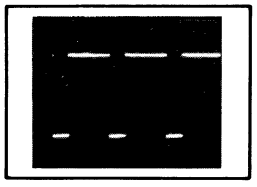
6 5V/DIV, 20μs/DIV



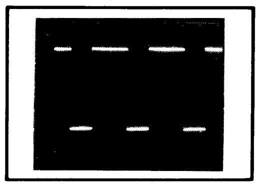
7 2V/DIV, 20μs/DIV



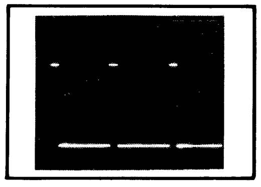
8 2V/DIV, 20μs/DIV



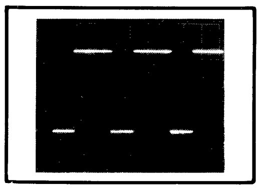
9 2V/DIV, 20μs/DIV



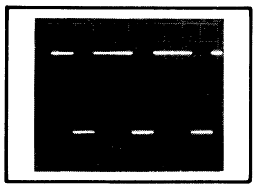
10 2V/DIV, 5ms/DIV



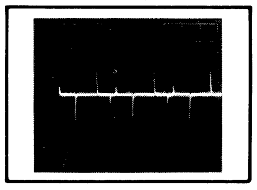
11 2V/DIV, 5ms/DIV



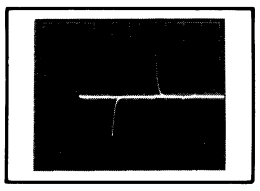
12 2V/DIV, 5ms/DIV



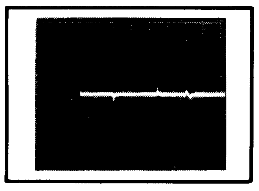
13 50mV/DIV, 20μs/DIV



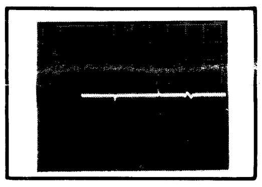
14 0.2V/DIV, 10μs/DIV



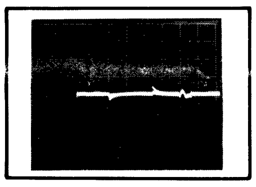
15 20mV/DIV, 10μs/DIV



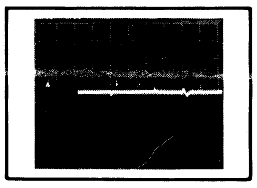
16 20mV/DIV, 10μs/DIV



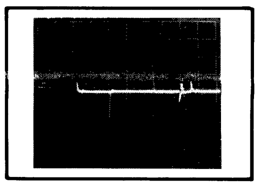
17 20mV/DIV, 10μs/DIV



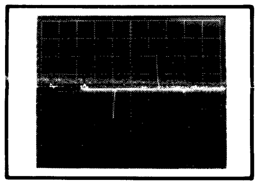
18 20mV/DIV, 10μs/DIV



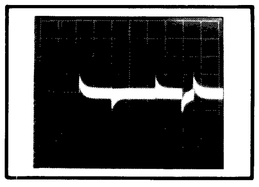
19 50mV/DIV, 10μs/DIV



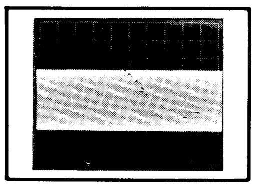
20 0.1V/DIV, 10μs/DIV



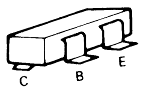
21 20mV/DIV, 10μs/DIV



22 1V/DIV, 10μs/DIV



2SB709-QRS
2SD601-QRS
2SD602-QRS
UN2217TW



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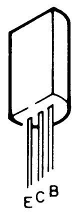
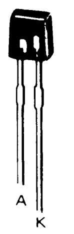
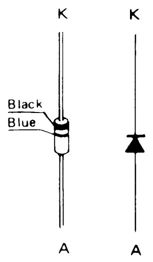


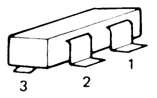
SEL1121R



1SS99

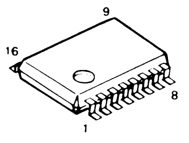

K
K
Black
Blue
A
A

MA151A



1 : Cathode
2 : Cathode
3 : Anode

HD14572UBP
TC4053BF
TC4538BF



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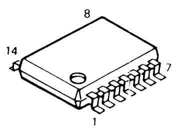

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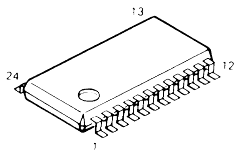

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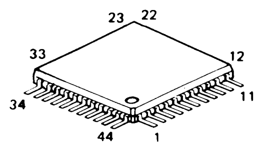
23 22
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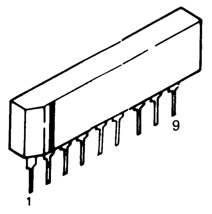
AN6913



ORDER NO. VKD84110883S8

Service Manual

Colour Video Camera
WV-555 Series

Supplement-3

Panasonic
WV-555
Panasonic

CONTENTS

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3. REPLACEMENT PARTS LIST 12

- Please file this supplement-2 service manual with original service manual (Order No. VKD83100784C8).

Panasonic

Matsushita Electric Trading Co., Ltd.
P.O. Box 288, Central Osaka Japan

1. ADJUSTMENT PROCEDURES

1-1 Deflection and High Voltage AIC Board

- Adjustment procedures of Rotation adjustment between (a) Target voltage adjustment and (b) Focus adjustment on page 13 for 4-5 Deflection and High Voltage AIC Board Adjustment have been added.

(a) Rotation adjustment

Adjust	: Tube rotation
Observe	: Monochrome underscanned video monitor

- Set OVERSCAN SWITCH on the Deflection board to the OVERSCAN position.
- Connect the PIX/GEN-LOCK connector on the rear of camera to the monochrome underscanned video monitor.
- Set the Monitor/PIX Select Switch to the R-G position.
- Connect the capacitor 100μF 10V to TP2(R) on Process-2 board (+ lead) and ground (- lead).
- Disassemble the camera as previously described in Section 3 Pick-up Tube Replacement on page 4.

- G rotation adjustment

- Loosen the G tube holding ring. (Fig. 1)

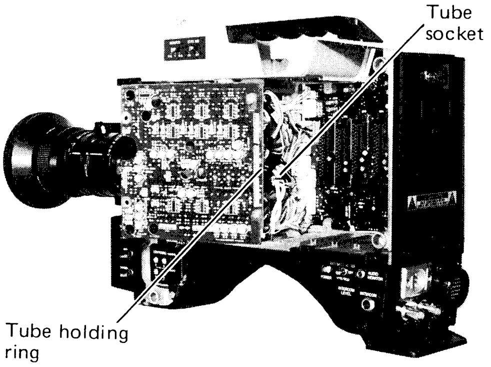


Fig. 1

- Rotate the G tube by means of the tube socket and stop at the point where the bottom of picture EDGE and the bottom of monitor edge becomes horizontally. (Fig. 2)

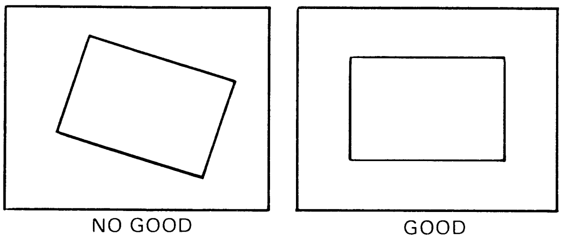

NO GOOD
GOOD

Fig.2

- Tighten the G tube holding ring.

- R rotation adjustment

- Disconnect the capacitor 100μF 10V to TP2(R) on Process-2 board and ground.
- Loosen the R tube holding ring. (Fig. 3)

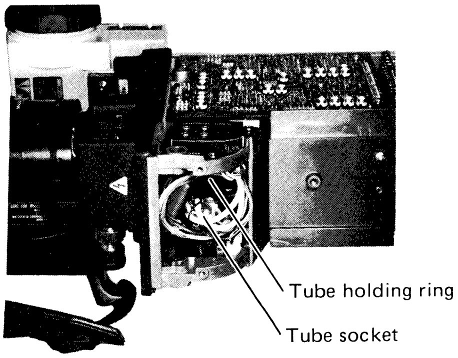
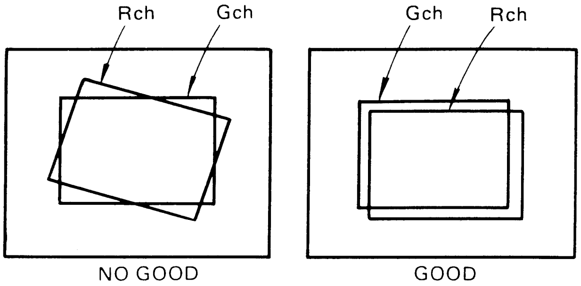


Fig. 3

- Rotate the R tube by means of the tube socket so that the R picture coincide with the G picture. (Fig. 4)



NO GOOD
GOOD

Fig. 4

- Tighten the R tube holding ring.

- B rotation adjustment

- Set the Monitor/PIX Select Switch to the B-G position.
- Loosen the B tube holding ring. (Fig. 5)

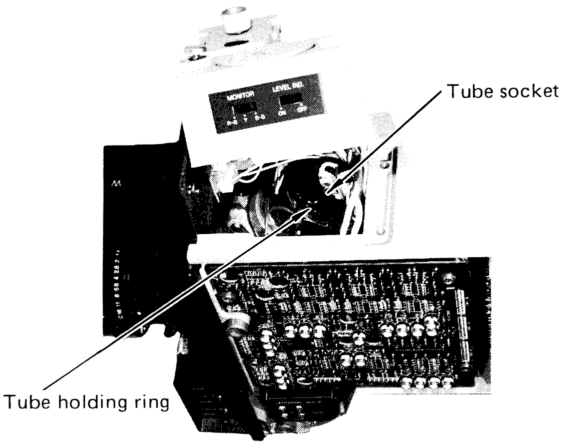
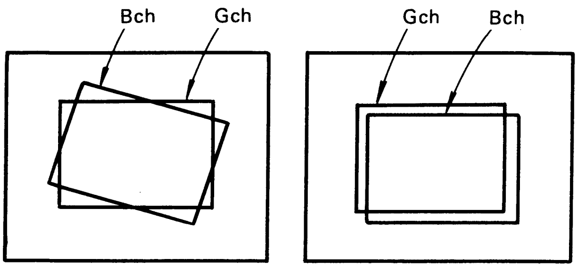


Fig. 5

- Rotate the B tube by means of the tube socket so that the B picture coincide with the G picture. (Fig. 6)



NO GOOD GOOD

Fig. 6

- Tighten the B tube holding ring.

1-2 Detail Board

- **The underline passages of (c) Detail (aperture) noise suppress adjustment on page 27 and (e) Detail gain adjustment on page 28 for 4-8 Detail Board Adjustment have been changed.**

(c) Detail (aperture) noise suppress adjustment

Test point :	TP2 (DETAIL OUT)	Detail board
Adjusts :	VR4 (DETAIL NOISE SUPPRESS)	Detail board
	VR5 (DETAIL GAIN)	Detail board
	VR3 (LEVEL DEPENDENT)	Detail board

- Connect the oscilloscope to TP2 (DETAIL OUT) and trigger the oscilloscope at H rate (Use TP8 (HD), Mother board.)
- Set the monitor/PIX Select Switch to the Y position.
- Aim the camera at the logarithmic gray scale chart and set the lens iris to F2.8.
- Turn DETAIL GAIN VR5 to its mechanical center and LEVEL DEPENDENT VR3 fully clockwise.
- Turn DETAIL NOISE SUPPRESS VR4 fully clockwise to release the suppression and note the noise level. (Fig. 4-8-4)

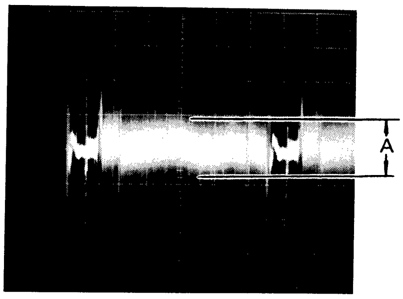


Fig. 4-8-4

- Adjust DETAIL NOISE SUPPRESS VR4 so that the noise level is 2/3A. (Fig. 4-8-5)

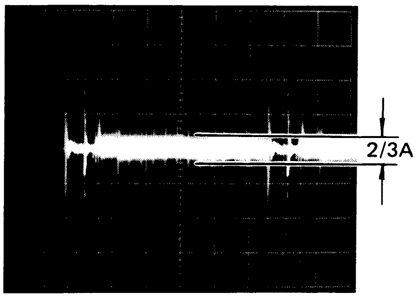


Fig. 4-8-5

(e) Detail gain adjustment

Test point :	VIDEO OUT	
Adjusts :	VR5 (DETAIL GAIN)	Detail board
	VR6 (H DETAIL GAIN)	Detail board

- Set the Monitor/PIX Select Switch to the Y position.
- Aim the camera at the window chart.
- Set the lens iris to Y signal becomes 0.46V.
- Connect the oscilloscope to the terminated VIDEO OUT signal or connect the VIDEO OUT to the waveform monitor.
- Trigger the oscilloscope at V rate. (Use TP7(VD), Mother board.)
- Adjust DETAIL GAIN VR5 so that the vertical detail (aperture) signal is 25% higher than the Y signal A. (Fig. 4-8-7)

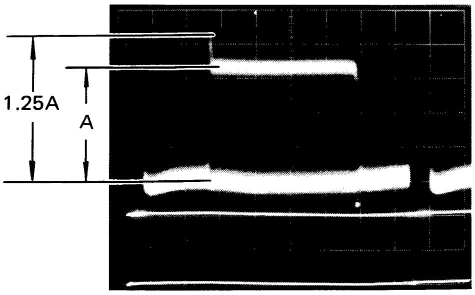


Fig. 4-8-7

- Trigger the oscilloscope at H rate. (Use TP8(HD), Mother board.)
- Adjust H DETAIL GAIN VR6 so that the horizontal detail (aperture) signal (B+C)/2 is 15% higher than the Y signal A. (Fig. 4-8-8)

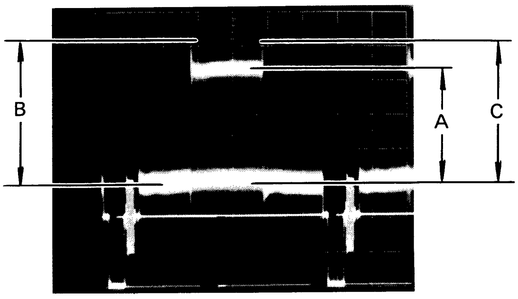


Fig. 4-8-8

1-3 Process-2 Board

- **The underline passages of (a) G gamma pedestal and gain adjustment on page 28 for 4-9 Process-2 Board Adjustment are corrected.**

Test points :	TP1 (G)	Process-2 board
	TP4 (G)	Process-2 board
	VIDEO OUT	
Adjusts :	VR5 (G GAMMA)	Process-2 board
	VR6 (G GAIN)	Process-2 board
	VR4 (G PEDESTAL)	Process-2 board

- Aim the camera at the logarithmic gray scale chart and set the lens iris to F2.8.
- Connect the oscilloscope to TP1(G) and trigger the oscilloscope at H rate (Use TP8(HD), Mother board).
- Adjust G GAMMA VR5 so that the gray scale waveform is straight. (Fig. 4-9-1)

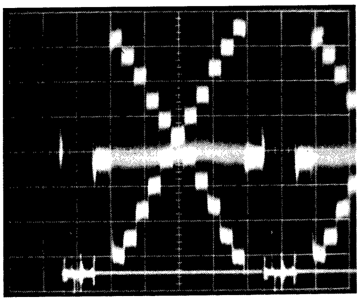


Fig. 4-9-1

- Cap on the lens or set the filter wheel to the position 4
- Connect the oscilloscope to TP4 (G).
- Turn G PEDESTAL VR4 clockwise to observe the signal as shown in Fig. 4-9-3. Turn VR4 back until the pedestal level is zero (The blanking level just touches to the noise.). (Fig. 4-9-3)

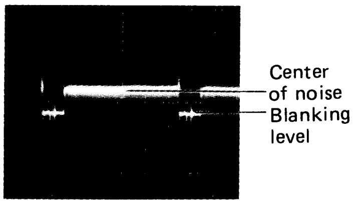


Fig. 4-9-2

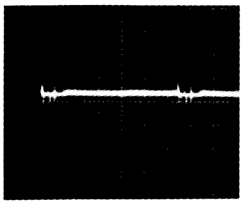


Fig. 4-9-3

Note: Confirm that the G pedestal level does not change by operating High Gain Selection Switch to 0dB and +12dB position.
If change, readjust the G BL OFFSET VR17 on Process-1 board.

- Set the lens iris to F2.8 and aim the camera at the gray scale.
- Connect the oscilloscope to terminated with 75 ohms VIDEO OUT connector.
- Adjust G GAIN VR6 so that the signal level between the blanking level and the top step of gray scale waveform is 0.7V. (Fig. 4-9-4)

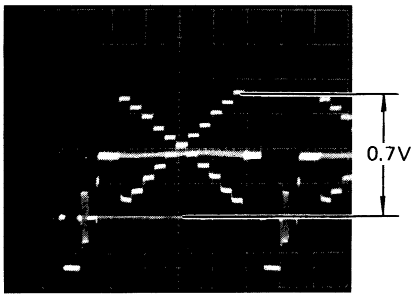
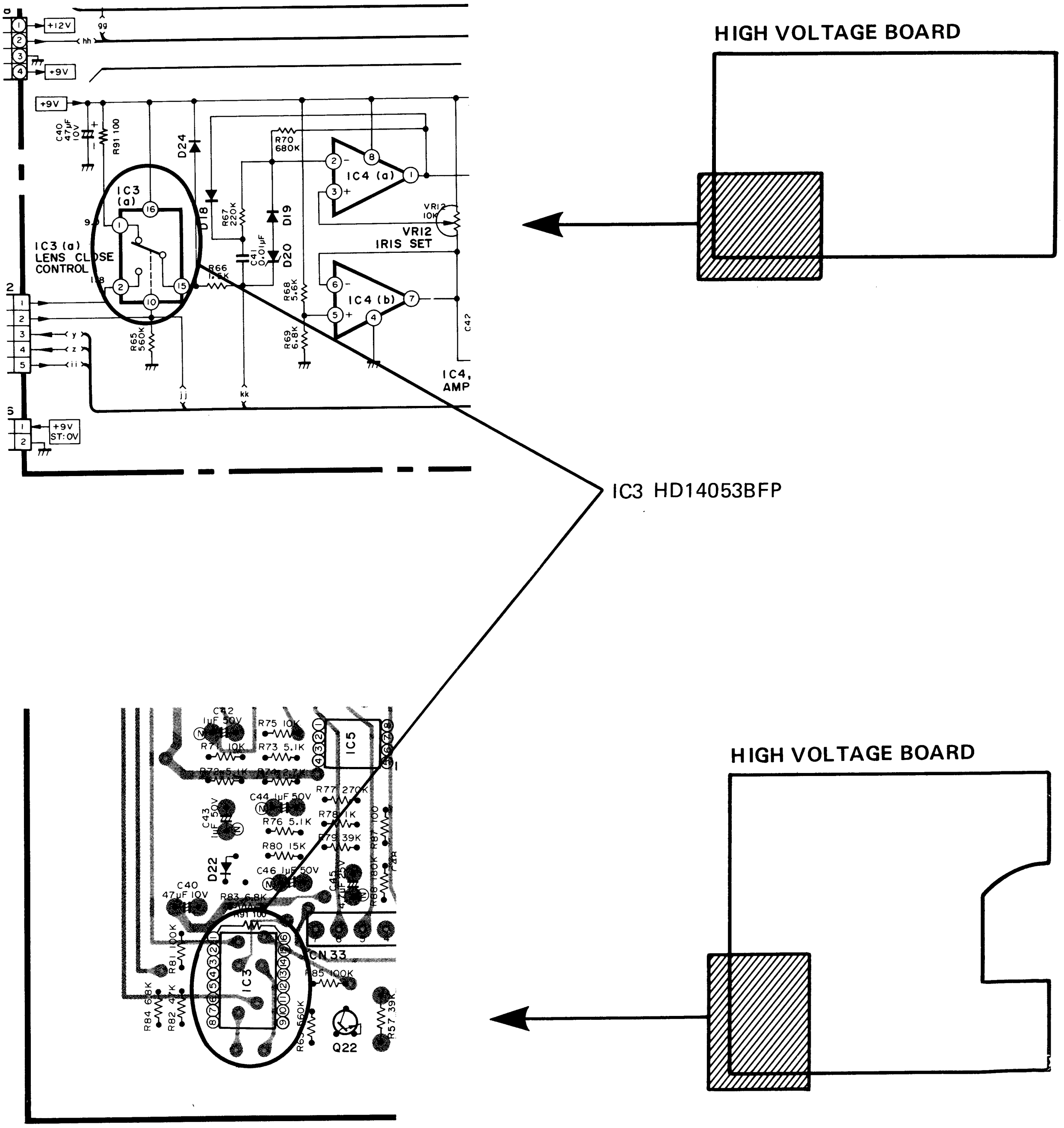


Fig. 4-9-4

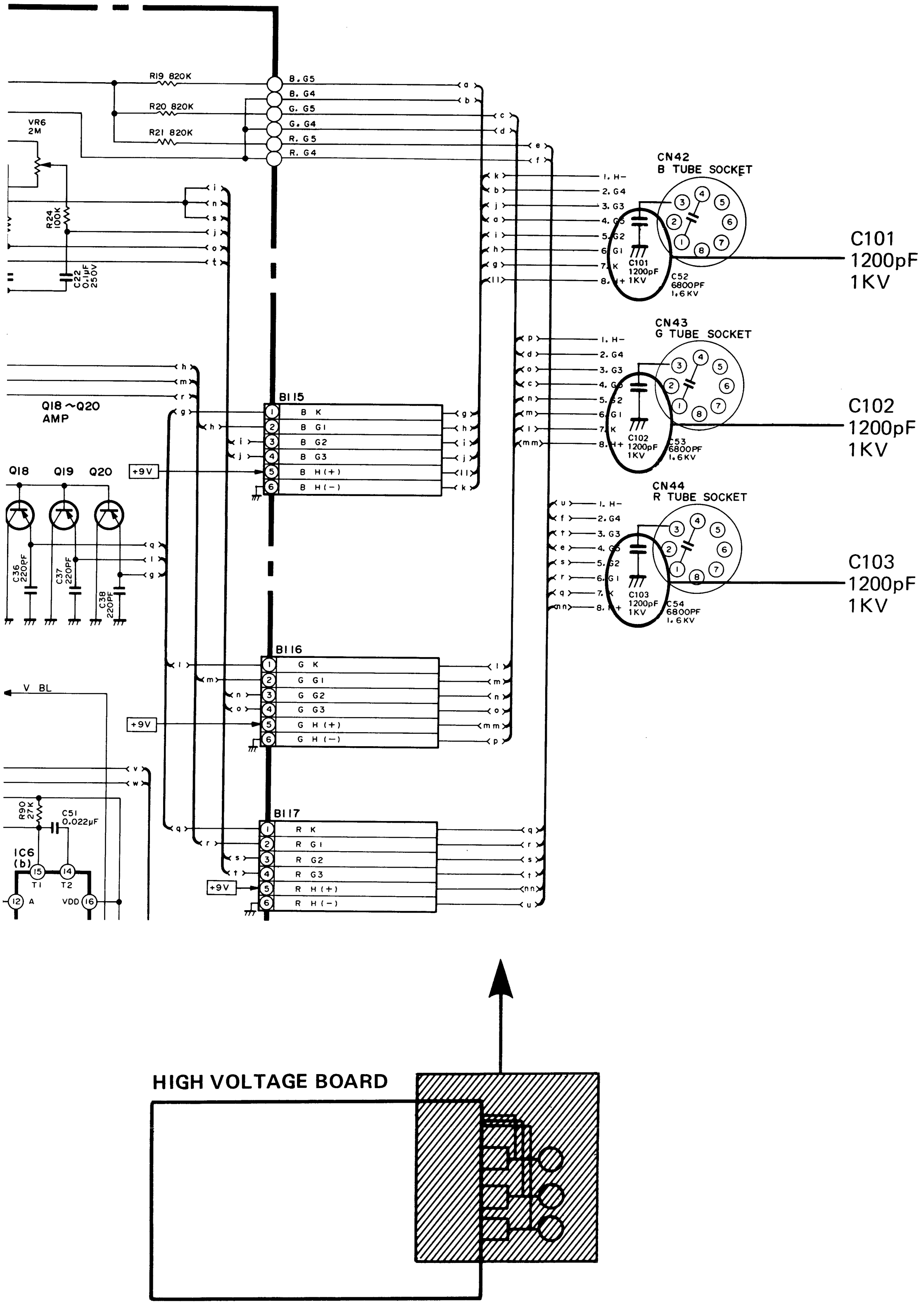
2. SCHEMATIC DIAGRAM and CONDUCTOR VIEWS

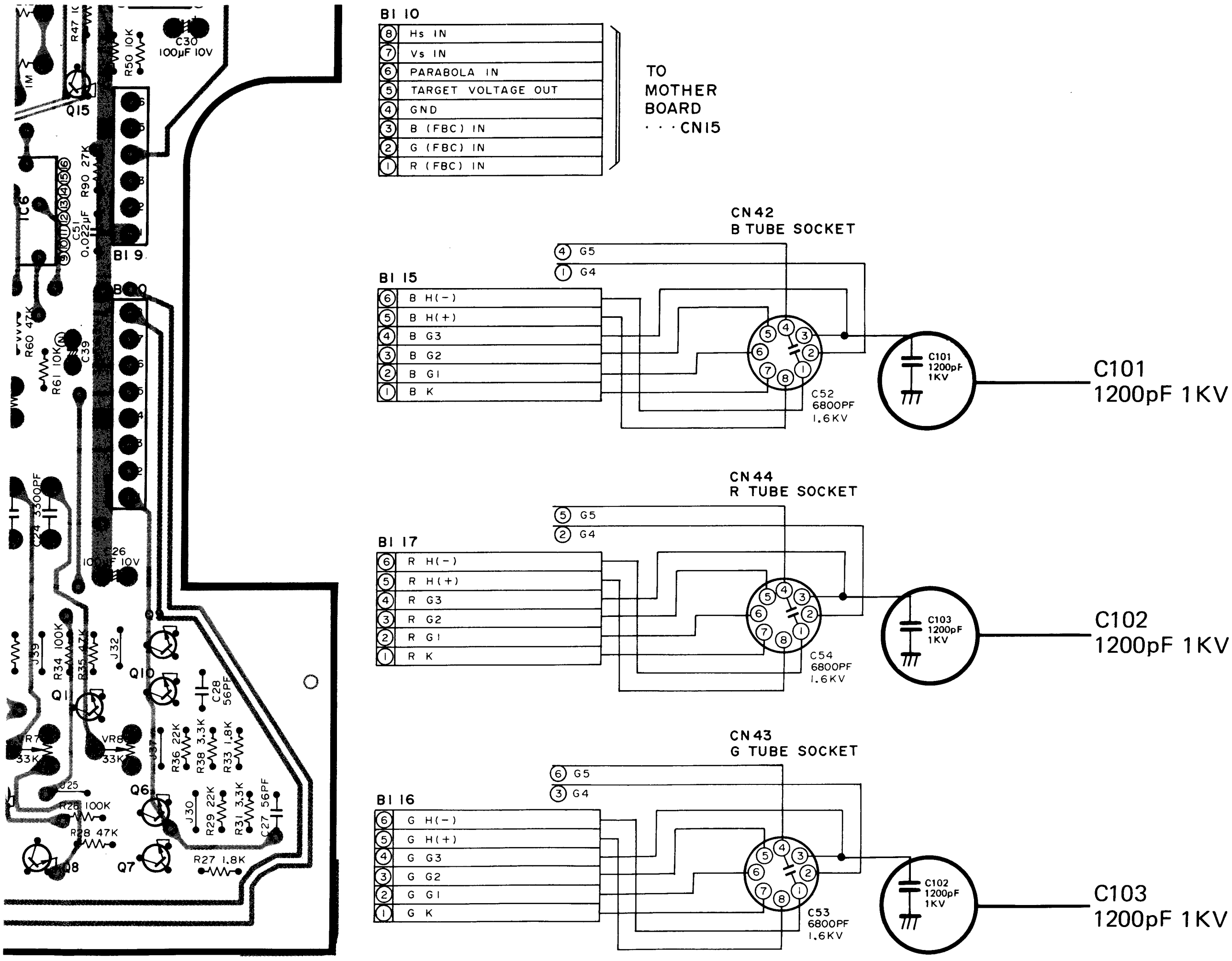
2-1 High Voltage AIC Board

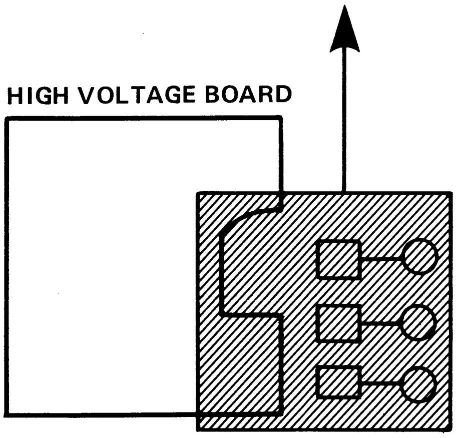
- IC3 on the High voltage AIC board have been changed to prevent the latch-up current from serial No. 46A00001 and higher.
- IC3 has been changed from TC4053BF to HD14053BFP.


HIGH VOLTAGE BOARD
+12V
+9V
ST:0V
C40 47µF 10V
R91 100
D24
IC3 (a)
IC3 (a) LENS CLOSE CONTROL
R65 560K
R66
R67 220K
R70 680K
D18
D19
D20
C41 0.01µF
R68 5.6K
R69 6.8K
IC4 (a)
IC4 (b)
VR12 10K
VR12 IRIS SET
C42
IC4, AMP
IC3 HD14053BFP
HIGH VOLTAGE BOARD
C42 1µF 50V
R75 10K
R71 10K
R73 5.1K
R72 5.1K
R74 2.7K
IC5
C44 1µF 50V
C43 1µF 50V
R77 270K
R78 1K
R76 5.1K
R79 39K
R80 15K
R87 100
R88 180K
D22
C46 1µF 50V
C45
C40 47µF 10V
R83 6.8K
R91 100
R81 100K
R84 6.8K
R82 47K
IC3
CN33
R85 100K
R65 560K
Q22
R57 39K

- C101, C102 and C103 on Tube socket have been changed to improve the RF interference from serial No. 45A00001 and Higher.

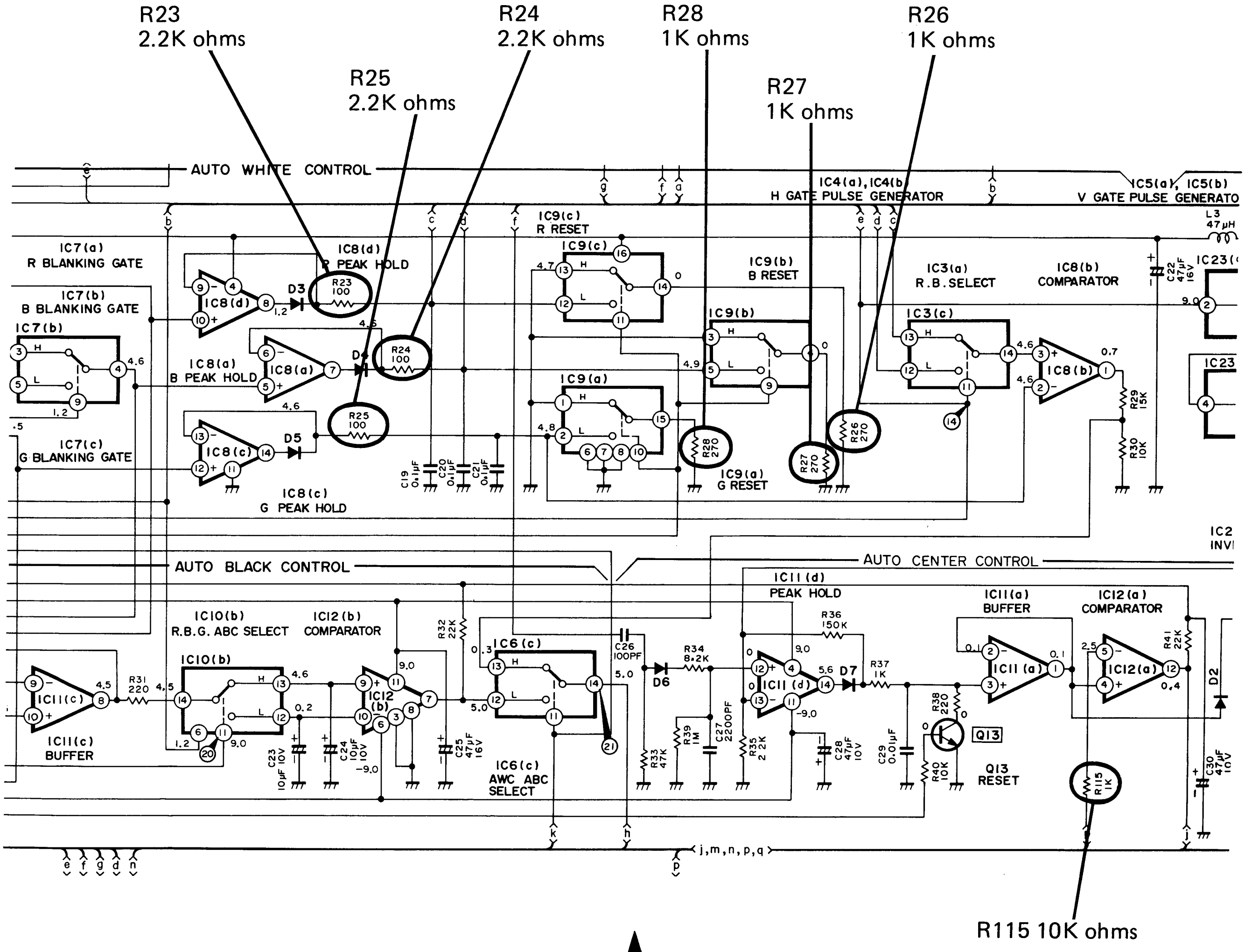

R19 820K
R20 820K
R21 820K
VR6 2M
R24 100K
C22 0.1μF 250V
B. G5
B. G4
G. G5
G. G4
R. G5
R. G4
CN42
B TUBE SOCKET
1. H-
2. G4
3. G3
4. G5
5. G2
6. G1
7. K
8. H+
C101 1200pF 1KV
C52 6800PF 1.6KV
C101
1200pF
1KV
CN43
G TUBE SOCKET
C102 1200pF 1KV
C53 6800PF 1.6KV
C102
1200pF
1KV
CN44
R TUBE SOCKET
C103 1200pF 1KV
C54 6800PF 1.6KV
C103
1200pF
1KV
Q18 ~Q20
AMP
Q18
Q19
Q20
+9V
C36 220PF
C37 220PF
C38 220PF
B115
B K
B G1
B G2
B G3
B H(+)
B H(-)
B116
G K
G G1
G G2
G G3
G H(+)
G H(-)
B117
R K
R G1
R G2
R G3
R H(+)
R H(-)
V BL
R90 27K
C51 0.022μF
IC6 (b)
T1
T2
A
VDD
HIGH VOLTAGE BOARD

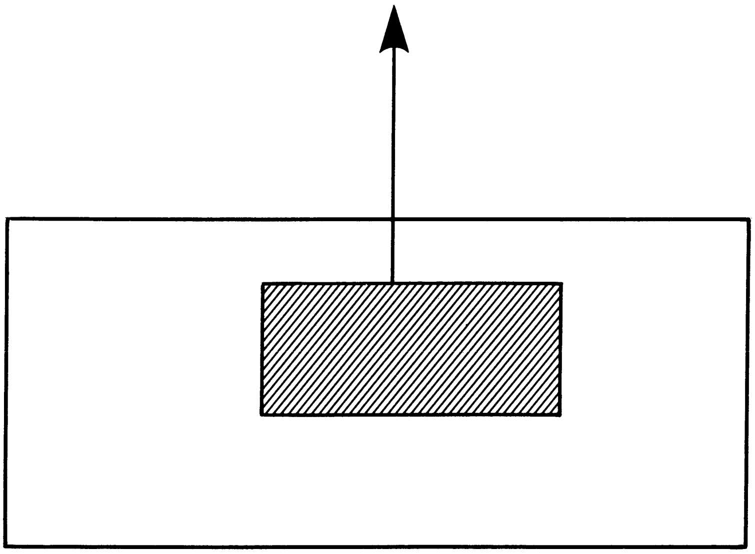

B1 10
⑧ Hs IN
⑦ Vs IN
⑥ PARABOLA IN
⑤ TARGET VOLTAGE OUT
④ GND
③ B (FBC) IN
② G (FBC) IN
① R (FBC) IN
TO MOTHER BOARD ···CN15
CN42
B TUBE SOCKET
④ G5
① G4
B1 15
⑥ B H(−)
⑤ B H(+)
④ B G3
③ B G2
② B G1
① B K
C52 6800PF 1.6KV
C101 1200pF 1KV
C101
1200pF 1KV
CN44
R TUBE SOCKET
⑤ G5
② G4
B1 17
⑥ R H(−)
⑤ R H(+)
④ R G3
③ R G2
② R G1
① R K
C54 6800PF 1.6KV
C103 1200pF 1KV
C102
1200pF 1KV
CN43
G TUBE SOCKET
⑥ G5
③ G4
B1 16
⑥ G H(−)
⑤ G H(+)
④ G G3
③ G G2
② G G1
① G K
C53 6800PF 1.6KV
C102 1200pF 1KV
C103
1200pF 1KV
R47
R50 10K
C30 100μF 10V
Q15
IC6
R90 27K
C51 0.022μF
B1 9
B1 10
R60 47K
R61 10K
C39
C24 3300PF
C26 100μF 10V
J39
R34 100K
R35 47K
J32
Q9
Q10
C28 56PF
Q1
R7 33K
VR8 33K
J31
R36 22K
R38 3.3K
R33 1.8K
J25
R26 100K
R28 47K
Q6
J30
R29 22K
R31 3.3K
C27 56PF
Q8
Q7
R27 1.8K


HIGH VOLTAGE BOARD

2-2 Auto Board

- The auto white control circuit on the Auto board has been changed to prevent the drift of auto white balance at bright object in edge from serial No. 46A00001 and higher.


R23
2.2K ohms
R24
2.2K ohms
R28
1K ohms
R26
1K ohms
R25
2.2K ohms
R27
1K ohms
R115 10K ohms
AUTO WHITE CONTROL
IC4(a),IC4(b)
H GATE PULSE GENERATOR
IC5(a), IC5(b)
V GATE PULSE GENERATO
IC7(a)
R BLANKING GATE
IC7(b)
B BLANKING GATE
IC7(c)
G BLANKING GATE
IC8(d)
R PEAK HOLD
IC8(a)
B PEAK HOLD
IC8(c)
G PEAK HOLD
IC9(c)
R RESET
IC9(b)
B RESET
IC9(a)
G RESET
IC3(a)
R.B.SELECT
IC8(b)
COMPARATOR
AUTO BLACK CONTROL
AUTO CENTER CONTROL
IC10(b)
R.B.G. ABC SELECT
IC12(b)
COMPARATOR
IC11(c)
BUFFER
IC6(c)
AWC ABC
SELECT
IC11(d)
PEAK HOLD
IC11(a)
BUFFER
IC12(a)
COMPARATOR
Q13
RESET

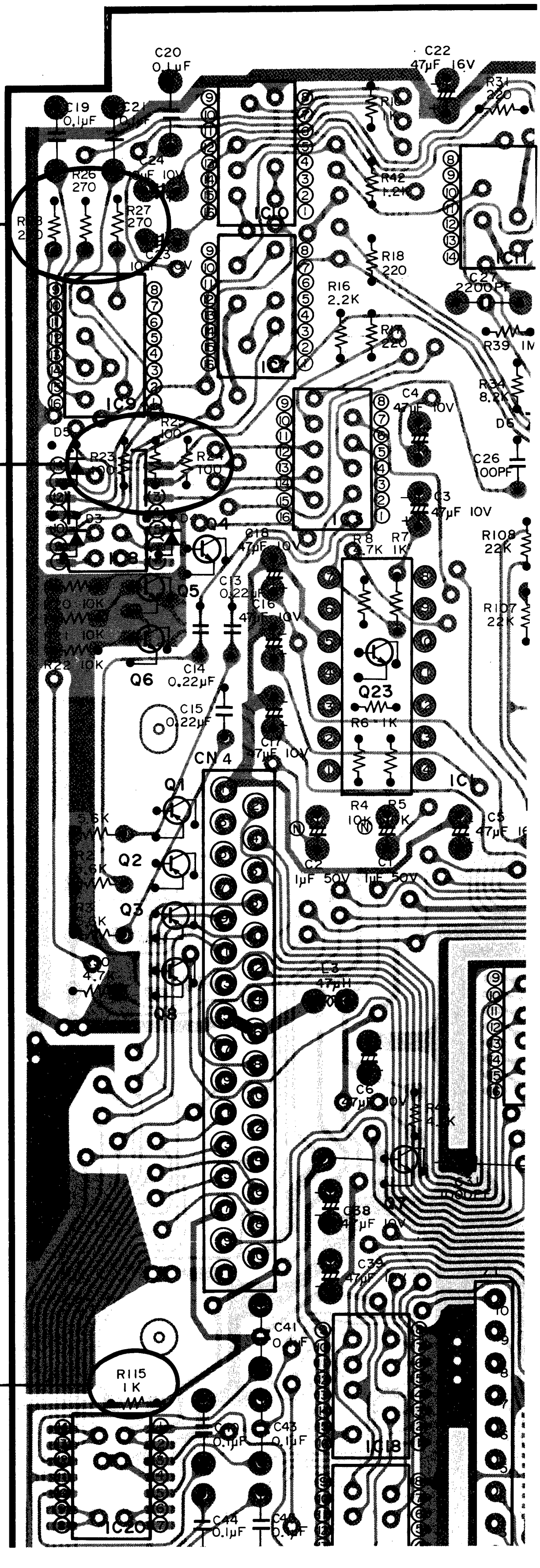


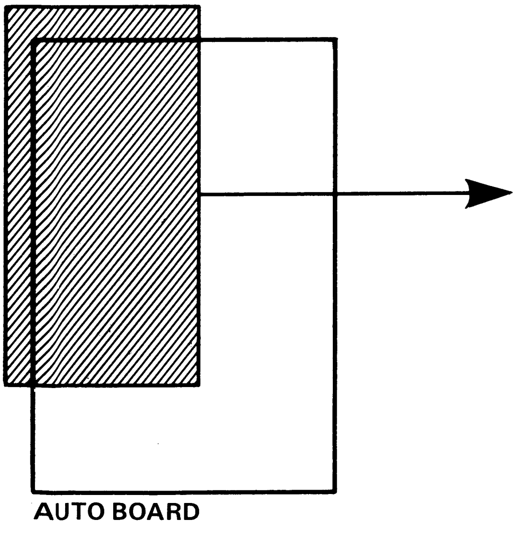
AUTO BOARD

R26 1K ohms
R27 1K ohms
R28 1K ohms

R23 2.2K ohms
R24 2.2K ohms
R25 2.2K ohms

R115 10K ohms

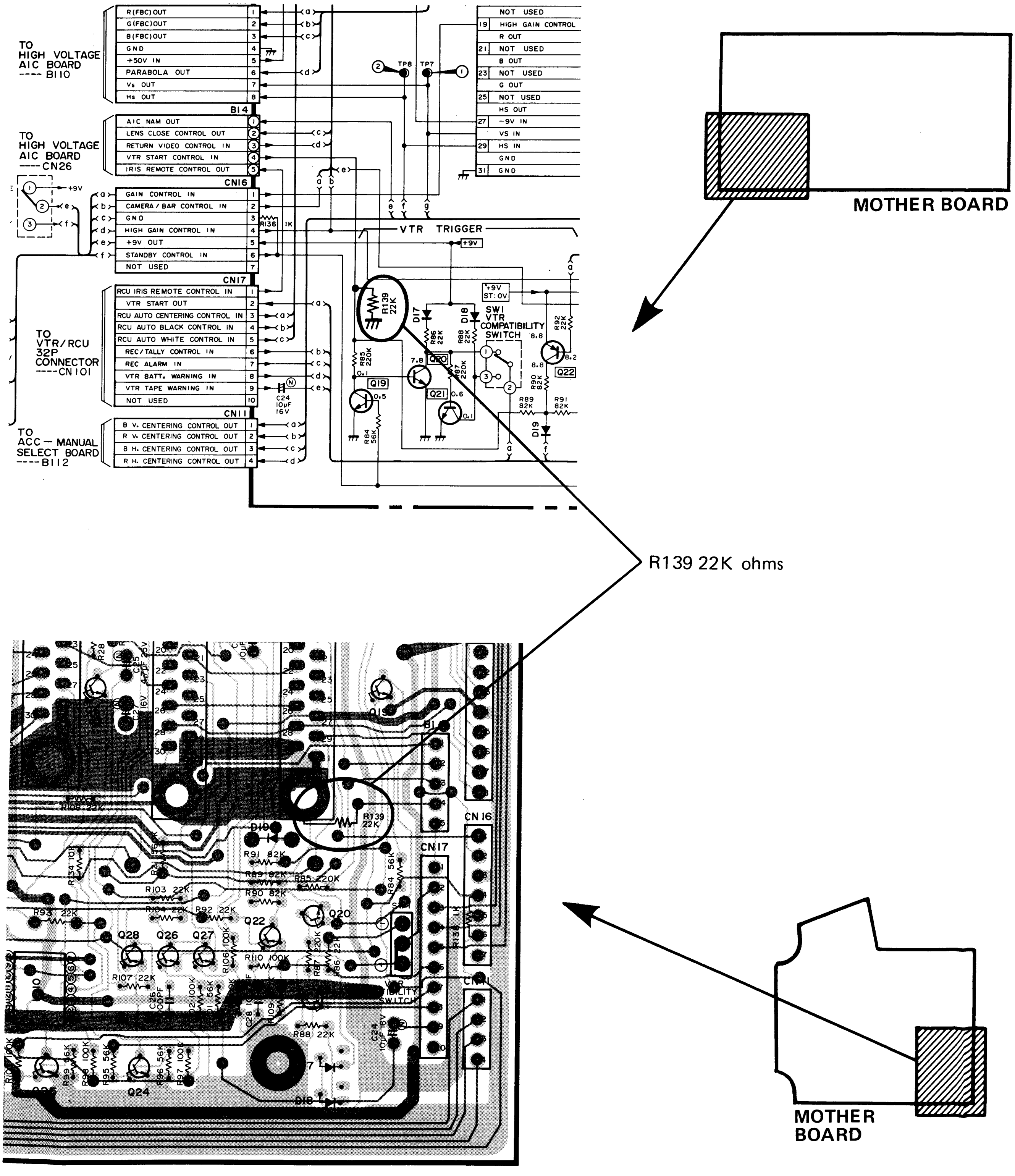

C20
0.1μF
C22
47μF 16V
R31
220
C19
0.1μF
C21
0.1μF
C24
10V
R26
270
R27
270
R28
270
C23
10V
R19
1K
R42
1.2K
IC10
R18
220
R16
2.2K
R17
220
C27
2200PF
R39
R34
8.2K
IC11
IC9
IC7
D5
R23
100
R24
100
R25
100
C4
47μF 10V
D6
C26
100PF
C3
47μF 10V
R108
22K
R107
22K
IC8
Q4
C18
47μF 10V
Q5
C13
0.22μF
C16
47μF 10V
R8
4.7K
R7
1K
Q23
R6 1K
R20 10K
R21 10K
R22 10K
Q6
C14
0.22μF
C15
0.22μF
C17
47μF 10V
CN4
Q1
Q2
Q3
Q8
R4
10K
R5
1K
C5
47μF
C2
1μF 50V
C1
1μF 50V
L3
47μH
C6
47μF 10V
C38
47μF 10V
C39
47μF 10V
C41
0.1μF
R115
1K
C42
0.1μF
C43
0.1μF
C44
0.1μF
IC20
IC18



AUTO BOARD

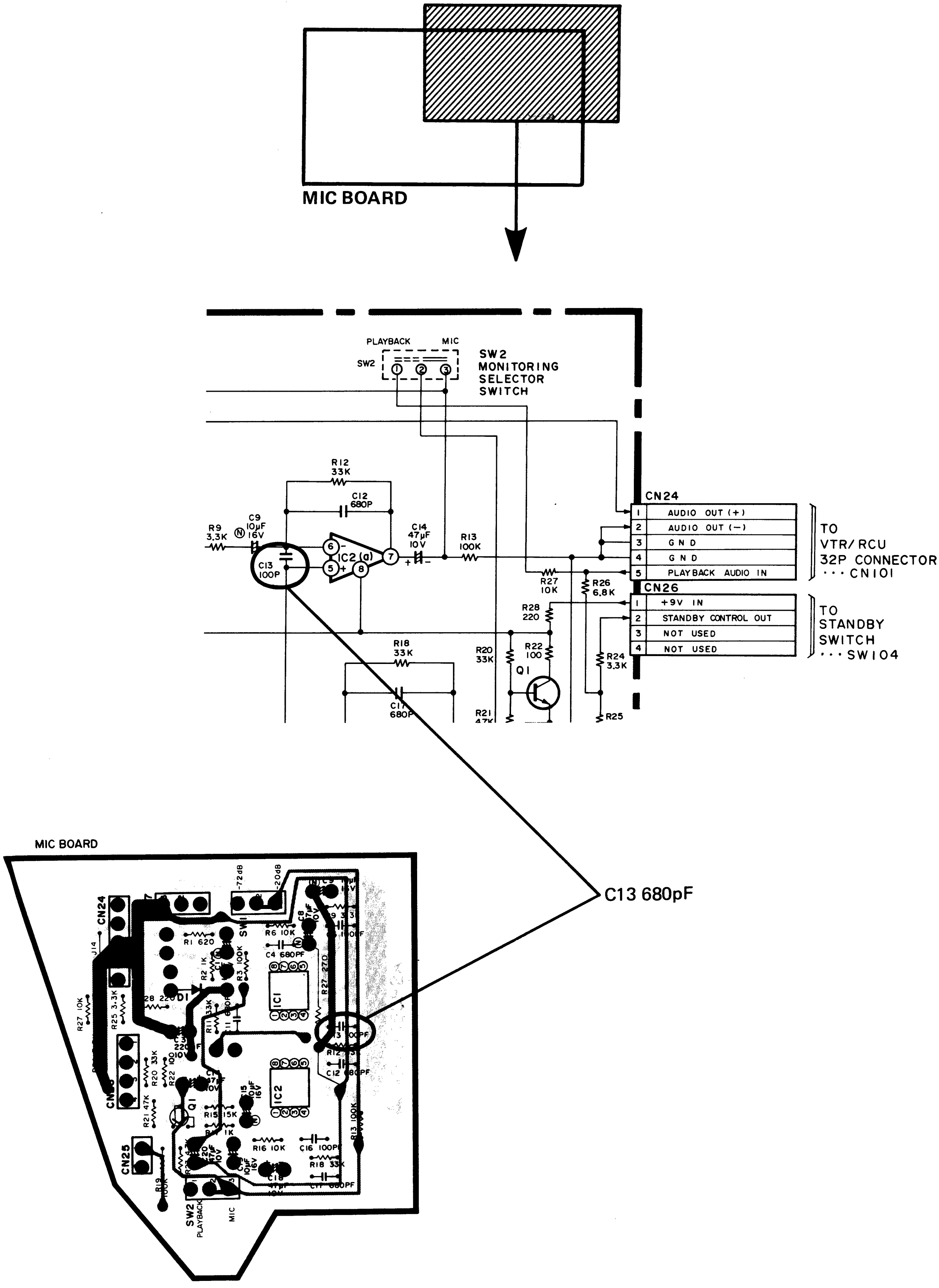
2-3 Mother Board

- R139 on the Mother board has been added to improve the VTR trigger of movement speed from serial No. 47A00001 and higher.


TO HIGH VOLTAGE AIC BOARD ----B110
R(FBC)OUT
G(FBC)OUT
B(FBC)OUT
GND
+50V IN
PARABOLA OUT
Vs OUT
Hs OUT
B14
TO HIGH VOLTAGE AIC BOARD ----CN26
AIC NAM OUT
LENS CLOSE CONTROL OUT
RETURN VIDEO CONTROL IN
VTR START CONTROL IN
IRIS REMOTE CONTROL OUT
CN16
GAIN CONTROL IN
CAMERA / BAR CONTROL IN
GND
HIGH GAIN CONTROL IN
+9V OUT
STANDBY CONTROL IN
NOT USED
CN17
TO VTR/RCU 32P CONNECTOR ----CN101
RCU IRIS REMOTE CONTROL IN
VTR START OUT
RCU AUTO CENTERING CONTROL IN
RCU AUTO BLACK CONTROL IN
RCU AUTO WHITE CONTROL IN
REC/TALLY CONTROL IN
REC ALARM IN
VTR BATT. WARNING IN
VTR TAPE WARNING IN
NOT USED
CN11
TO ACC – MANUAL SELECT BOARD ----B112
B V. CENTERING CONTROL OUT
R V. CENTERING CONTROL OUT
B H. CENTERING CONTROL OUT
R H. CENTERING CONTROL OUT
NOT USED
HIGH GAIN CONTROL
R OUT
NOT USED
B OUT
NOT USED
G OUT
NOT USED
HS OUT
-9V IN
VS IN
HS IN
GND
GND
TP8
TP7
R136 1K
VTR TRIGGER
+9V
R139 22K
D17
D18
R86 22K
R88 22K
R85 220K
R87 220K
Q19
Q20
Q21
Q22
R84 56K
C24 10μF 16V
+9V ST: 0V
SW1 VTR COMPATIBILITY SWITCH
R92 22K
R90 82K
R89 82K
R91 82K
D19
MOTHER BOARD
R139 22K ohms
R139 22K
CN16
CN17
CN11
D19
R91 82K
R89 82K
R85 220K
R90 82K
R84 56K
R103 22K
R104 22K
R92 22K
R93 22K
Q28
Q26
Q27
Q22
Q20
Q19
R110 100K
R107 22K
R88 22K
Q24
VTR COMPATIBILITY SWITCH
MOTHER BOARD

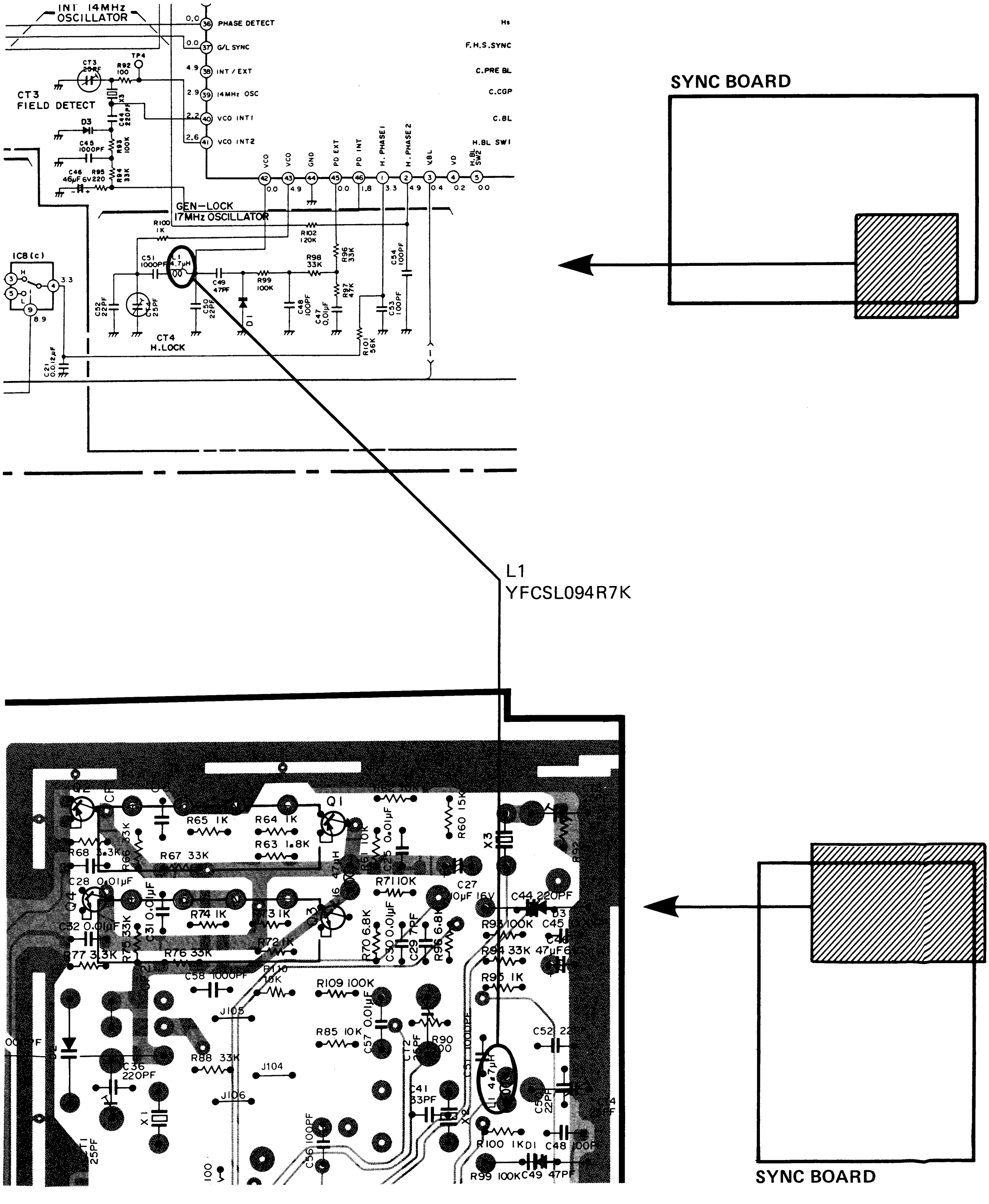
2-4 Mic Board

- C13 on the Mic board has been changed to prevent the oscillation of mic amp circuit from serial No. 48A00001 48A00001 and higher.


MIC BOARD
PLAYBACK
MIC
SW2
SW2 MONITORING SELECTOR SWITCH
R12 33K
C12 680P
R9 3.3K
C9 10μF 16V
C13 100P
IC2(a)
C14 47μF 10V
R13 100K
CN24
1 AUDIO OUT (+)
2 AUDIO OUT (−)
3 GND
4 GND
5 PLAYBACK AUDIO IN
TO VTR/RCU 32P CONNECTOR ···CN101
R27 10K
R26 6.8K
CN26
1 +9V IN
2 STANDBY CONTROL OUT
3 NOT USED
4 NOT USED
TO STANDBY SWITCH ···SW104
R28 220
R22 100
Q1
R18 33K
R20 33K
C17 680P
R21 47K
R24 3.3K
R25
C13 680pF
MIC BOARD
CN24
CN25
SW2
PLAYBACK
MIC
IC1
IC2
Q1
D1
R1 620
R6 10K
C4 680PF
R16 10K
C16 100PF
R18 33K
R13 100K
R27 10K
R25 3.3K
R21 47K
R20 33K

2-5 Sync Board

- L1 on the Sync board has been changed to prevent the drift of H. SYNC LOCK from serial No. 47A00001 and higher.
- L1 has been changed from YFL54R7J to YFCSLO94R7K.


INT 14MHz OSCILLATOR
PHASE DETECT
G/L SYNC
INT / EXT
14MHz OSC
VCO INT1
VCO INT2
CT3 FIELD DETECT
GEN-LOCK 17MHz OSCILLATOR
CT4 H.LOCK
IC8 (c)
SYNC BOARD
L1
YFCSL094R7K
SYNC BOARD

3. REPLACEMENT PARTS LIST

SYMBOL NO.	ORIGINAL PARTS NO.	NEW PARTS NO.	DESCRIPTION		
PCB12 HIGH VOLTAGE AIC BOARD					
IC103	TC4053BF	**HD14053BFP**	IC		
C101	–	**YFB3AD152M**	Plastic	1200pF	1000V
C102	–	**YFB3AD152M**	Plastic	1200pF	1000V
C103	–	**YFB3AD152M**	Plastic	1200pF	1000V

PCB14 AUTO BOARD					
R23	ERJ8GCSJ101	**ERJ8GCSJ222**	Carbon	2.2K ohms	1/8W
R24	ERJ8GCSJ101	**ERJ8GCSJ222**	Carbon	2.2K ohms	1/8W
R25	ERJ8GCSJ101	**ERJ8GCSJ222**	Carbon	2.2K ohms	1/8W
R26	ERJ8GCSJ271	**ERJ8GCSJ102**	Carbon	1K ohms	1/8W
R27	ERJ8GCSJ271	**ERJ8GCSJ102**	Carbon	1K ohms	1/8W
R28	ERJ8GCSJ271	**ERJ8GCSJ102**	Carbon	1K ohms	1/8W
R115	ERJ8GCSJ102	**ERJ8GCSJ103**	Carbon	10K ohms	1/8W

PCB7 MOTHER BOARD					
R139	–	**ERJ8GCSJ223**	Carbon	22K ohms	1/8W

PCB2 MIC BOARD					
C13	YF426101CHJS	**YF42651SLJ**	Ceramic	680pF	50V

PCB10 SYNC BOARD					
L1	YFL54R7J	**YFCSL094R7K**	Coil	4.7μH	